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# A New electronic image array: The Active pixel charge injection device

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A NEW ELECTRONIC IMAGE ARRAY: THE ACTIVE PIXEL CHARGE  
INJECTION DEVICE

by  
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Diploma in Electronics and Telecommunications Engineering,  
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A dissertation submitted in partial fulfillment of the  
requirements for the degree of Doctor of Philosophy  
at the Center for Imaging Science,  
Rochester Institute of Technology

November 2002

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CHESTER F. CARLSON CENTER FOR IMAGING SCIENCE  
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CERTIFICATE OF APPROVAL

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Ph.D. DEGREE DISSERTATION

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The Ph.D. Degree Dissertation of George S. Lungu has been examined  
and approved by the dissertation committee as satisfactory for the  
dissertation requirement for the Ph.D. degree in Imaging Science

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A NEW ELECTRONIC IMAGE ARRAY: THE ACTIVE PIXEL CHARGE  
INJECTION DEVICE

by  
George Lungu

Submitted to the  
Chester F. Carlson Center for Imaging Science  
College of Science  
in partial fulfillment of the requirements  
for the degree of Doctor of Philosophy  
at the Rochester Institute of Technology

**Abstract**

This is a Ph.D. thesis dissertation in which a new type of image sensor is investigated as possible successor to the charge coupled device (CCD) for scientific applications.

As a result of the work described in this dissertation, the active pixel charge injection device (AP-CID) has been developed. This device retains most of the positive features of both the charge injection device (CID) imager (random readout, non-destructive readout, antiblooming, increased UV sensitivity, radiation tolerance, low

power consumption, low manufacturing price) and the CCD imager (low noise, high dynamic range). The device lacks most of the drawbacks of the aforementioned devices.

A functional array architecture was created. Based on this architecture several devices were fabricated. One of the arrays was fully measured, characterized and suggestions for improvement were formulated. Most of the characterization/analysis work described in this dissertation was centered on the following issues: *temporal noise*, *linearity* and *FPN*.

The measured noise performance of the new device is excellent and comparable to the noise performance of the scientific CCD.

The newly developed sensor is necessary for scientific imaging applications in space based operation. However due to its qualities, this device could be used in a much wider range of applications including commercial digital cameras, spectroscopy, biological, nuclear and other scientific applications.

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I acknowledge Dr. Zoran Ninkov who was the person who originally accepted me into the Ph.D. program, providing a goal and training in solid state sensors; providing funding and advice. He was also the person who recommended me to work for CIDTEC (Spectra Physics) as a way of improving my knowledge in the field.

I would like to thank Joe Carbone for hiring me at CIDTEC, offering training in sensors and allowing me access to state of the art technology.

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# Chapter 1. Solid State Imaging Arrays Background

## 1.1. Historical perspective

In the 1960's there were numerous groups working on solid state image sensors with varying degrees of success using PMOS, NMOS or the bipolar process. For instance, in 1963 Morrison<sup>1</sup> reported a structure called *junction photopot* that allowed determination of a light spot's position using the photoconductivity effect. The main advantage of this kind of device was speed (which was limited only by the minority carrier lifetime). In the same paper Morrison describes a similar two-dimensional device called the *junction scanner*.

In 1964, IBM<sup>2</sup> reported the *scanistor*. It used an array of phototransistors addressed through a resistive network to produce an output pulse proportional to the local incident light intensity.

In 1966, Westinghouse and NASA reported a 50 x 50 element monolithic array of phototransistors<sup>3</sup>. All of these sensors reported so far were working in an instantaneous light to output signal conversion mode. As a consequence, the sensitivity of these devices was low.

In 1967, Weckler at Fairchild suggested using a p-n junction in a photon-flux-integrating mode. The photocurrent from the junction was integrated on a reverse biased p-n junction capacitance. The signal charge, appearing as a current pulse, could be converted to a voltage pulse by using a resistor. A simple method for eliminating the dark current effects in the measurement was described, by differentially reading out two identical junctions, one of them being placed in the dark.

In 1968, Dyck and Weckler report a 100x100-element photodiode array<sup>4</sup>. Each pixel contained both, a bipolar and a MOS transistor. The photodiode was actually the emitter-base junction of the bipolar transistor. The MOS transistor was simply a row selection switch. The sensitivity of this solid state imager outpaced about one order of magnitude the sensitivity of a typical Vidicon tube. Weckler later called the device a *reticon*.

In 1967, Weimar<sup>5</sup> reported a thin film transistor (TFT) solid-state image sensor using CdS/CdSe complementary transistors and photoconductive films. Noble, in 1968 described a self-scanned silicon detector array<sup>6</sup>. Both, surface photodiodes and buried photodiodes (dark current reduction) were used. A charge integration amplifier was described, and for the first time a source follower buffer in each pixel was reported. This architecture is very similar to a modern APS architecture. Chamberlain reported an improved model and description of the sensor operation<sup>7</sup> in 1969. He also described the design and measured performance of shift registers, integrated as drivers on the same chip.

Fry, Noble and Rycroft explored the issue of fixed pattern noise (FPN) in a 1970 paper<sup>8</sup>. Until recently FPN has been considered the most important problem related to MOS active pixel imagers.

In 1970 when the CCD was first reported<sup>9</sup>, its relative freedom from FPN was the main reason for its adoption over the many other forms of solid state image sensors<sup>13</sup>. A CCD is an analog shift register and it can also be used for applications different than imaging.

Since its invention there have been impressive improvements in the CCD technology driven especially by the camcorder market. There have been few reports about merging the CCD and CMOS technologies, but overall, the subject proved to be unfruitful because the amount of heat dissipated by the CCD driving electronics was very large. The extra steps required for making a CMOS process from a CCD process would also diminish the performance of the CCD process itself.

While a large effort was applied to the development of the CCD, Japanese companies continued the development of the MOS image sensors<sup>10,11</sup> in the late 1970's and early 1980's. In 1982, a single-chip MOS color imager was reported<sup>12</sup>.

The early 1990's brought resurgence in CMOS image sensor development. Three separate research groups are important to mention here: one in Scotland at the University of Edinburgh, one in Sweden at Linkoping University and one at the U.S. Jet Propulsion Laboratory. The research of the last group was prompted by NASA's need for highly miniaturized, low-power, radiation-hard, instrument imaging systems for next generation deep-space exploration spacecraft<sup>13</sup>.

### **1.1.1. Timeline of the AP-CID development at RIT**

The milestones in developing the AP-CID device at RIT are the following:

- June 1998 – the first active pixel array (8x8 RIT AP-CID) was successfully fabricated at RIT and tested based on a design by G Lubberts.
- August 1998 - the second active pixel array (54x40 RIT AP-CID) was successfully designed, fabricated and tested at RIT, together with G. Lubberts.
- November 1998 – the design of the third active pixel array (128x128 Orbit AP-CID) was completed.
- March 1999 – the fabrication of the third array was completed. The array was tested and proved to be functional. The first images with an AP-CID array were obtained.
- June 2000 – the design of the fourth array (6x32x32 Mosis AP-CID) was completed. The fabricated device was not functional due to a design error.
- August 2001 – the design of the 388x16 Orbit AP-CID was completed.
- February-November 2002 – the last array was being successfully measured and characterized. The results are presented in this thesis.

## 1.2. Basics on solid state imaging

### 1.2.1. Photo-generation of electric charge in silicon

When a photon with energy greater than the energy band-gap  $E_g$  of the semiconductor is absorbed into the depletion region of a MOS capacitor a free electron-hole pair is created. This is known as the *photoelectric effect*.

$$E_{\text{photon}} \geq E_g \quad (1.1)$$

$$E_{\text{photon}} = h \cdot \nu_{\text{photon}} = \frac{h \cdot c}{\lambda_{\text{photon}}} \quad (1.2)$$

where  $h$  is Plank's constant,  $\nu$  is the frequency,  $\lambda$  is the wavelength and  $c$  is the speed of light. An important observation can be made that there is a *critical wavelength* beyond which photo-generation doesn't occur. The critical wavelength is related to the semiconductor band-gap by the following formula,

$$\lambda_c = \frac{hc}{E_g} = \frac{1.24}{E_g \text{ (eV)}} [\mu\text{m}] \quad (1.3)$$

For intrinsic silicon  $E_g = 1.12$  eV and  $\lambda_c = 1.1 \mu\text{m}$ . For extrinsic silicon, energy levels can exist within the forbidden region, reducing the effective band-gap, thus increasing the critical wavelength. A first order approximation is the assumption that any photon with wavelength shorter than  $\lambda_c$  produces one electron-hole pair.

After photo-generation, the minority carrier will be driven to the surface potential minimum and the majority carrier will move into the substrate. This way, an isolated potential well will contain charge, which is proportional to the time integral of the incident optical or infrared flux.

### ***1.2.1.1 Types of non-linearity in the conversion process***

There exist modifications in the above model for CCD sensors, which degrade the efficiency of the light-to-charge conversion. The number of signal charge carriers created per incident photon is called *quantum efficiency* ( $\eta$ ) or *spectral response*. Quantum efficiency is one of the most important parameters used to evaluate the quality of a photodetector and for special devices it can be greater than one. The quantum efficiency depends on several factors such as:

***Absorption coefficient* ( $a$ )** – the absorption of the light in a solid can typically be described by Beer's law:

$$I(x) = I_0 \cdot e^{-a \cdot x} \quad (1.4)$$

where  $I(x)$  represents the light irradiance at the distance  $x$  from the surface. The absorption coefficient relates to the probability of how far into a material an incident photon will travel in average before being absorbed by the lattice producing ionization. Absorption coefficient is expressed in units of  $\text{cm}^{-1}$ . The shorter wavelength (higher energy) photons are absorbed nearer to the material's surface than the longer wavelength photons. If the absorption coefficient is too high or too low, the minority carrier can be produced in a region where it cannot be collected as usable signal, therefore reducing quantum efficiency.

***Recombination lifetime* ( $\tau$ )** – the photo-induced minority charge carrier density decays in time by recombination. The time constant for this process is called the *recombination lifetime*  $\tau$ . The recombination can take place by two mechanisms. The direct transition of a carrier between the valence band and the conduction band yielding a photon is a

mechanism not very probable in silicon material. More probable is a heat generating indirect recombination mechanism, which occurs through intermediate states between the conduction and the valence band. These states are generated by impurities, phonons and lattice defects. Typically a sensor is built on a silicon wafer which has a “denuded zone” within the first few microns from the surface free from lattice defects, while the bulk is heavy populated with crystal defects and where the minority carrier lifetime is very short. Moreover, the minority carrier lifetime at the silicon surface is reduced due to a large number of defects (incomplete lattice bonds or dangling bonds) at the silicon to silicon dioxide interface. For the above reasons for both very short and very long wavelengths the quantum efficiency tends to drop.

**Diffusion length ( $L_n$ )** – Represents the average distance a photo-generated minority charge carrier can migrate before it recombines. A large value for this parameter renders higher quantum efficiency. The electric charge diffusion mechanisms in silicon will be treated later. However it should be mentioned that in a neutral substrate the recombination lifetime,  $\tau$ , and the electron diffusion length,  $L_n$  are related by:

$$L_n = \sqrt{D_n \cdot \tau} \quad (1.5)$$

where  $D_n$  is the diffusion coefficient for the minority carriers in question.

**Overlaying films** – in order to realize a functional CCD image sensor a stack of patterned thin film materials is created above the silicon surface. Typically, the materials are silicon oxide, polysilicon, silicon nitride, silicides, metals and color filter materials. Ideally these materials would need to be perfectly transparent over a wide range of wavelengths. From a practical standpoint, the electrode structure on the top of the silicon material presents a considerable absorption and reflectance, which is a function of wavelength. Polysilicon electrodes are transparent for optical wavelengths greater than 450 nm, so that they allow the light collection efficiency to be satisfactory except for a poor response in the blue region of the spectrum. If a good response is required throughout the entire visible



spectrum, the illumination can be made incident on the back surface of the device. A back illuminated CCD is built in a near conventional technology, except that at the end, a significant amount of the substrate is eliminated by etching and polishing. A distance of few tens of microns separates the silicon-oxide interface from the back end. This thickness has to be comparable with the electrode dimensions otherwise the random diffusion of charge carriers towards the storage sites will cause image blurring. This requirement usually ensures that the diffusion path is much shorter than the minority carrier diffusion length. If infrared detection is required the substrate must not be made too thin owing to the greater thickness of silicon required for photon absorption, so that the problem of image blurring by diffusion remains. Frontal illumination may well provide a better compromise in this case especially while combined with indium-tin oxide (ITO) transparent electrodes.

### 1.2.2. Electric charge storage in the MOS capacitor

The basic building block of a CCD is the Metal-Oxide-Semiconductor (MOS) capacitor, used both as a light sensing element and electrical charge storage element. A MOS silicon structure is shown on Figure 1.4(a). As any capacitor, it consists of two electrodes, separated by an insulator. One of the electrodes is the bulk silicon. A thin layer of silicon oxide (typically few tens of nanometers) serves as dielectric. The second electrode, referred to as *gate*, is placed on the top of the dielectric and is made out of metal or heavily doped polysilicon. The gate is held at a voltage  $V$  and the substrate is provided with an ohmic contact held at the ground (reference) potential.

Three MOS structure band diagrams for different gate voltages are shown in Figure 1.1(b, c, d) for a p-type silicon substrate<sup>14</sup>. The *accumulation* state is shown in Figure 1.1(b). The negative gate voltage bends the energy bands upwards and the majority carriers (holes) are attracted and accumulate at the silicon-dielectric interface. Applying a small voltage as in the Figure 1.1(c), the holes are repelled deep into the semiconductor substrate. A depletion region is created right below the dielectric-semiconductor interface, where the electron and hole concentrations are small compared to the hole concentration deep into the substrate. This is the *depletion* state of the MOS capacitor. Further increase of the gate voltage bends the energy bands still downwards, creating a potential well at the interface, and attracting minority carriers (electrons) to the surface. At a certain threshold voltage the electron concentration at the interface becomes equal to the hole concentration in the substrate. This is the onset of the *strong inversion* state, as shown in Figure 1.1(d). Any further increase of the gate voltage is followed by a proportional increase of the electron concentration in the surface layer at the silicon-oxide interface. This surface electric charge has a shielding effect on the bulk of the semiconductor. The electric field away from the surface will remain almost constant and

therefore the width of the depletion region will remain constant<sup>15</sup>. As an equivalent circuit the structure behaves similar to a regular capacitor having the gate oxide as dielectric.

The holes generated in the depletion region are repelled into the substrate and collected by the back ohmic contact. The photo-generated electrons are collected in a potential well created at the interface by the potential gradient. The surface potential decreases with an increase of the surface electron concentration and as a result, the potential well becomes shallower. With time, the thermally generated electron-hole pairs, constituting the *dark current*, tend to bring the system back to the quasi-equilibrium state with zero potential gradient, setting a time limit for which the MOS capacitor is inversion. The dark current is exponentially dependent on the temperature, so the inversion state can be extended by cooling the device.

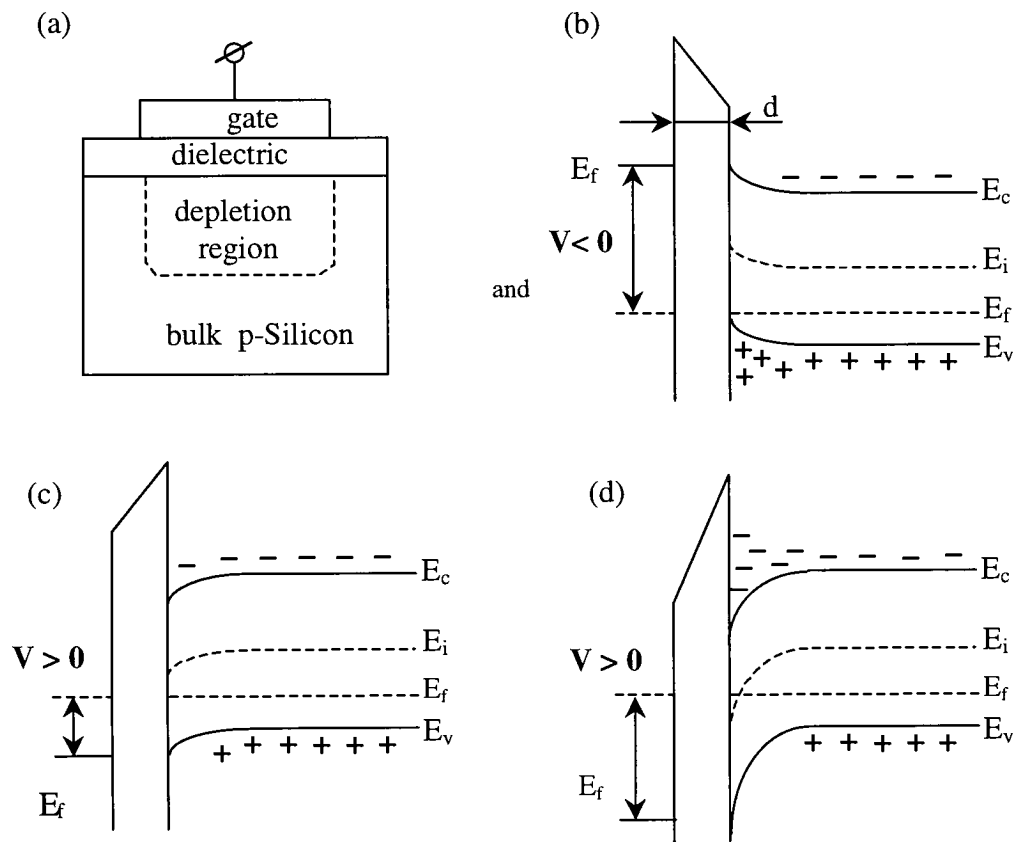


Figure 1.1 Basic MOS capacitor and its band diagrams

### 1.2.3. Electric charge transfer in semiconductors

The movement of charge packets of minority carriers through the silicon from one gate to another is realized by shaping and reshaping the potential wells under consecutive electrodes. Charge transfer in a CCD has to be fast and highly efficient. It is very important the efficiency at which the charge-transfer operation takes place. Any residual charge left behind when a transfer occurs will eventually join charge belonging to other pixels causing image blur. The maximum speed at which charge transfer occurs with a good efficiency will dictate the maximum readout speed of the CCD array. There are three distinct charge transfer mechanisms in a CCD as described by Carnes, Kosonocky and Ramberg<sup>16</sup>:

*-thermal diffusion of charge carriers* : even in the absence of any electric field a charge packet has the tendency to redistribute towards an equilibrium state.

*-self-induced fields* : if there is any charge concentration gradient, carriers of the same type will repel each other determining charge displacement until the gradient becomes zero.

*-fringing fields* : an electric field generated under the gate of a MOS structure can be associated to a potential well. For small dimensions of the potential wells while abutting gates at different potentials, the shape of a potential well will no longer be rectangular. Any deviation from a rectangular shape such as rounded edges or tilted bottom can be associated to an electric field component (called fringing field) parallel to the silicon surface. This component determines a flow (drift) of electric charge parallel to the oxide-silicon interface.

## 1.3. Main types of solid state imagers

### 1.3.1. The CCD

Till the end of the 1960's, the physical implementation of the active pixel image sensor had not been very successful due to the low-resolution lithographic techniques, the reduced yield and uniformity associated with the first integrated circuits. The concept of charge-coupled devices (CCD) was first presented in 1970 by Boyle and Smith<sup>9</sup>. The newly invented CCD eliminated the previously mentioned drawbacks of the early active pixel sensors.

#### *1.3.1.1. Charge storage and transfer*

A CCD is an analog shift register in which photo-generated charge can be stored, or carried along the surface in potential wells generated in semiconductor by an array of closely spaced MOS capacitors. Voltage levels applied on the metal electrodes control the charge position in the MOS array of capacitors. Under proper application of these voltage levels and their relative phases, the array can be used to store and transfer the photo-generated charge packets across the semiconductor substrate in a controlled manner. As an example, a P-surface channel CCD imager is presented. It is a one-dimensional four phase CCD array, which means that each pixel comprise a group of four MOS capacitors each connected to a different clock generator (phase). The four clocks are overlapping trapezoidal periodic pulses with the same frequency but different delays. They create a “moving well” effect which carries the photo-generated charge from pixel to pixel and prevents the mixing of the charge from different pixels. The charge is moved along a CCD channel laterally defined by two *channel stop* implant regions. Having the same type of doping, but much higher value than the substrate doping, these *channel stop*

regions cannot be inverted by the voltages on the gates. Therefore the corresponding potential wells in the channel stop regions will be shallow.

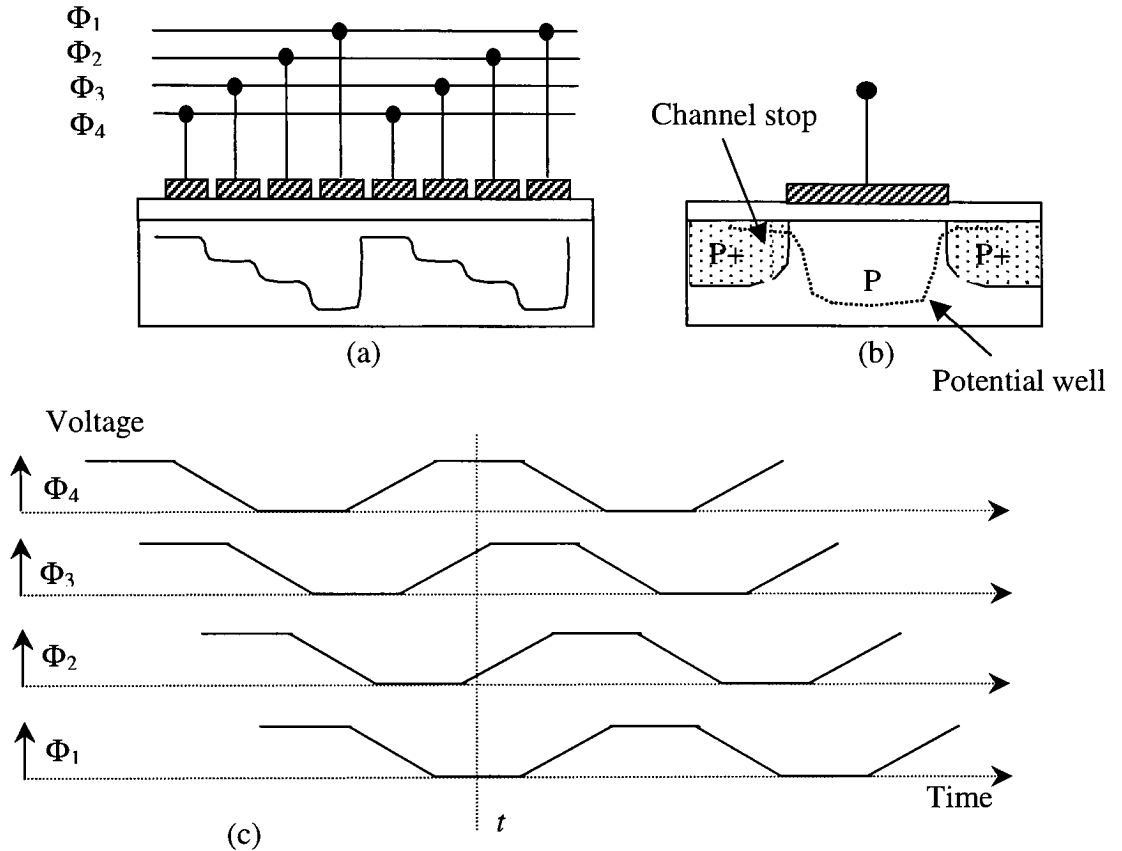


Figure 1.2 A longitudinal section through a four-phase CCD showing the electrode structure of two pixels and the respective potential wells within the silicon (a), a transversal section through the pixel showing the channel stops (b), and generic waveforms used to drive such a CCD. Note that the potential well structure represented in (a) corresponds to moment “t” in diagram (c)

### 1.3.1.2. Architecture

Only one of the numerous CCD architectures, which allow particular readout techniques to be employed, will be presented here. For a two-dimensional CCD array, a full-frame architecture is the simplest to fabricate and operate, hence yielding the highest resolution and pixel density. For this type of architecture, the pixels of the array are grouped in an  $m$ -wide ( $m$  being the number of columns) parallel shift register running vertically. At the bottom (end) of this parallel shift register the charge is transferred to a serial shift register having a length equal to the number of columns of the array. Therefore, to one charge transfer in the parallel register, correspond  $m$  transfers of the serial shift register. Because the parallel shift register is used for both scene detection and readout, a mechanical shutter is needed for this particular architecture.

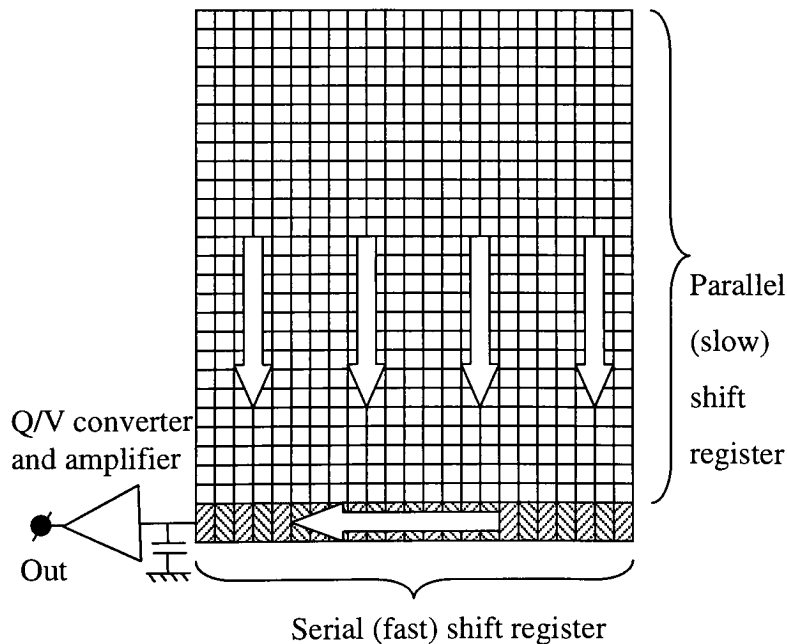


Figure 1.3 Full-frame CCD architecture

At the output of the fast shift register there is a charge-to-voltage converter typically followed by a floating diffusion and a MOS source follower as a voltage preamplifier. An illustration of this architecture is shown in Figure 1.3.

### 1.3.1.3. *The readout stage*

Figure 1.4 shows the schematic for the output stage of an N-channel CCD. The output stage of a CCD is a charge-to-voltage converter (floating diffusion) followed by a preamplifier, typically a source follower (transistor  $T_2$ ).

The CCD handles minority carriers. While the photogenerated majority carriers are repelled to the bulk by the electric field existent under the gate of a certain MOS structure (biased towards deep depletion), the corresponding minority carriers accumulate under the same gate in potential wells. This happens in every pixel, during light integration.

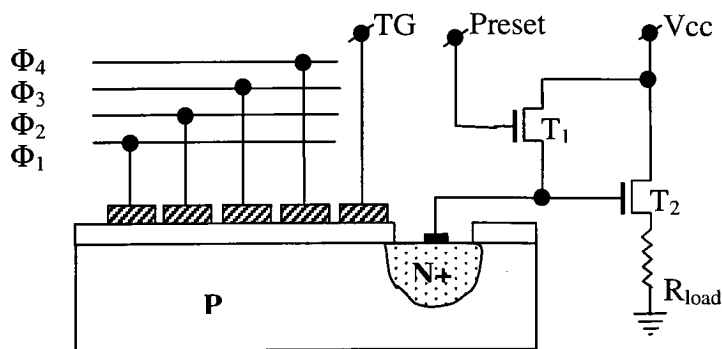


Figure 1.4 A typical CCD readout stage



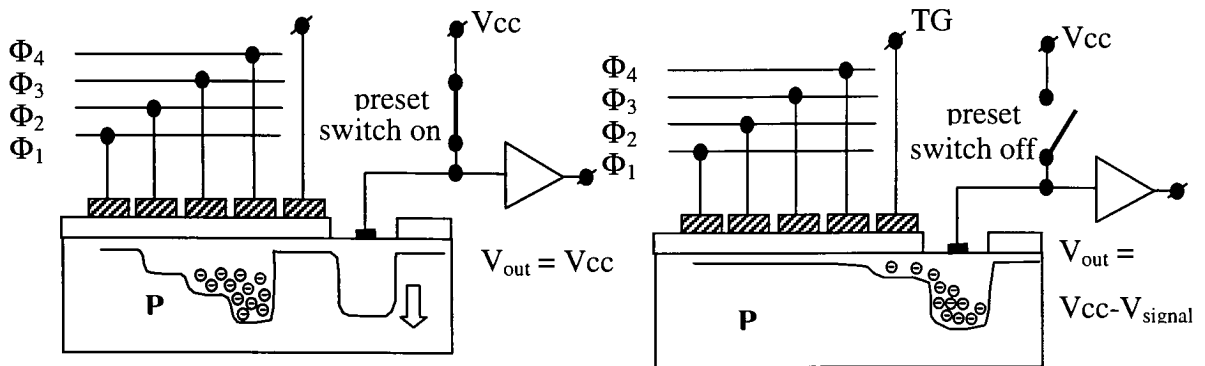


Figure 1.5 An illustration of the working principle for the output stage of a CCD. The *preset* phase (a) and the *charge-voltage* conversion phase (b).

By proper manipulation of the voltages on the array of gates, this charge is clocked towards the output in a serial fashion. The last gate, which is also called a *transfer gate* ends in a *floating diffusion*, i.e. a region of opposite doping type relative to the substrate. At the border between the substrate and the *floating diffusion*, a PN junction is formed.

The charge-to voltage conversion has two distinct phases. The first phase (Figure 1.5) is the *preset*, in which the junction is set to a reverse bias condition by closing a switch (transistor  $T_1$ ), and the *transfer gate* is *off* (biased in a weak depletion mode with the potential well collapsed underneath)

The second phase is the *charge-voltage conversion* when the diode is left floating and by turning the transfer gate *on*, allowing minority carriers to flow from the potential well corresponding to the last gate of the horizontal shift register to the floating diffusion. The built-in potential existent in the junction area will determine these carriers to flow towards the floating diffusion and reduce the preset voltage on the PN junction by a value proportional to the amount of this charge.

#### ***1.3.1.4. Advantages of the CCD imager***

**Noise:** The CCD array has the best noise among all the other categories of solid state imagers known today. Noise figures below one electron r.m.s. using multiple-read techniques have been reported. This low noise is determined by the fact that charge from each pixel is being driven to a unique output stage, which has a very high gain (voltage/charge) and is optimized for noise and linearity.

**Simplicity:** The CCD is the imager with the simplest pixel structure, and no driving circuitry necessary on chip.

**Size:** Very large size CCD imagers have been reported, some having more than 16 million pixels (Eastman-Kodak). Due to its simple structure, the pixel can be made as small as few times larger than the minimum feature size of the lithographic process used. In the beginnings of CCD technology, when the lithographic resolution was low, this was a great advantage allowing large format arrays to be built. Nowadays, when lithographic resolution is much below the pixel size of a typical CCD, the main factor, which prevents further increases in array size, is the charge transfer efficiency.

A significant advantage of the CCD that is important to mention is the very good spectral quantum efficiency of the back illuminated version of this type of imager. The back illuminated CCD however, is an expensive and rare device due to the low yield of the thinning operation.

#### ***1.3.1.5. Limitations of the CCD imager***

**Charge transfer inefficiency:** This limits the maximum array size, maximum speed, and maximum level of radiation a CCD imager of certain performance can tolerate.

***Nonrandom readout:*** Before reading a certain pixel, all the charge in the preceding pixels has to be moved to the readout node in a serial fashion. This seriously limits this type of imager in certain imaging applications such as fast tracking, fast image processing.

***Destructive readout:*** This makes the charge monitoring during exposure impossible.

***Large power required:*** The upper electrodes have a significant associated capacitance (typically tens of nanofarad per phase). The dynamic power required to drive a CCD is high.

***Quantum efficiency:*** For a front illuminated CCD the *quantum efficiency* is quite modest at short wavelengths (blue-UV), due to a sandwich of polysilicon/oxide layers stacked on the top of the bulk silicon. This sandwich represents nothing more than the array of electrodes and isolation among electrodes, and has a transmission coefficient, which degrades at short wavelengths. In order to overcome this problem, hybrid CCD-photodiode imagers are built.

***Blooming:*** It is the spill of photo-generated charge from saturated pixels to neighboring pixels. Unless a special structure (called an *overflow drain*) is placed in each pixel, a CCD is extremely susceptible to this effect<sup>17</sup>.

***Sensitivity to point defects:*** If a pixel has a high charge generation rate (due to a local defect or impurity), the electric charge transiting the pixel during the readout will be affected. From the image point of view, the effect of a point defect will not remain localized to a certain pixel<sup>17</sup>.

### 1.3.2. The charge injection device (CID) imager

The invention of the CID at General Electric<sup>18</sup> came two years after the invention of the CCD. The CID is typically a surface channel device that employs intra-cell charge transfer and charge injection into the substrate, to achieve the solid state image sensing function. Compared to the CCD, the CID brought into play advantages such as random readout, non-destructive readout, and resistance to radiation while maintaining a simple structure. Two different pixel structures will be analyzed here.

#### 1.3.2.1. Operation of the two-electrode pixel

The most common pixel architecture is the two-electrode X-Y addressable sensing site having two charge-coupled MOS capacitors.

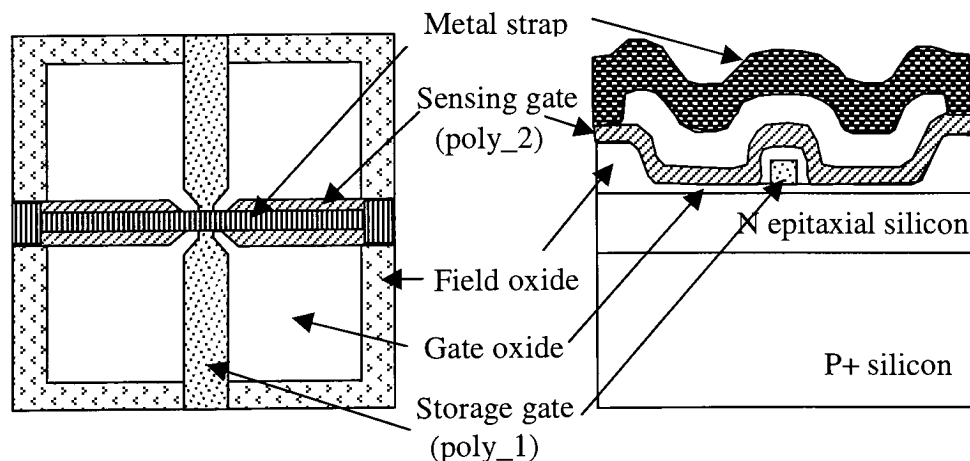


Figure 1.6 The layout of and a cross-section through a CID pixel

The basic approach is designing each capacitor such that one can store the signal charge when the other capacitor electrode is left electrically floating. Various methods can be used to couple surface charge between adjacent electrodes. Among these are fringing fields, which require a very narrow inter-electrode gap; overlapping but insulated electrodes; or the use of an interconnecting ion implanted region. The second method is the most common for the CID imagers fabricated to date.

Figure 1.6 shows an example of a P-channel CID pixel layout. The structure is built on a thin N-doped epitaxial layer (10-20 $\mu\text{m}$ ), grown on a heavily P-doped silicon wafer. Transparent row and column polysilicon electrodes are orthogonally placed over the layer of gate oxide and create two MOS capacitors. The *vertically running* electrode can be made up of *poly\_1* (the first deposited polysilicon layer). This electrode is called *column electrode* or *storage electrode*. The horizontally running electrode, made up of *poly\_2*, is called *row electrode* or *sensing electrode*. The two electrodes are electrically isolated due to a second layer of gate oxide grown on the top of the column electrode after this electrode was patterned. The width of the electrodes is reduced at the intersection point to diminish the crosstalk effects between the row and the column<sup>19</sup>.

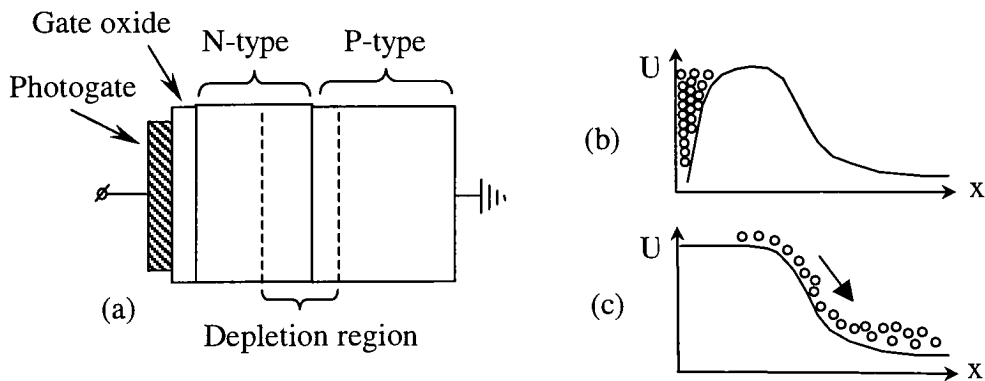


Figure 1.7 A cross section through a region of a CID pixel covered by photogate (a). The potential diagram of the MOS structure during inversion (b) and during injection (c). This particular device handles positive charge (holes in a P-channel).

An aluminum strip runs horizontally on the top of the sensing electrode, from one end of the array to the other, in order to minimize the row resistance, hence the readout noise<sup>20</sup>. The device is built on the top of a reverse biased vertical P-N junction. This structure provides antiblooming protection by having the excess minority carriers swept from the epitaxial layer to the substrate using the built-in electric field across the junction. Figure 1.7 shows a section through a CID pixel underneath a photogate, and the potential diagram for the case of charge storage and charge injection. There are four distinct stages in the operation of a typical CID imager. These stages are illustrated in Figure 1.8.

In the first stage (*light integration/preset*), both electrodes are biased at a negative potential, larger than the threshold in absolute value. Potential wells are created under both electrodes, but the sensing electrode (right side) has a shallower potential well underneath than the storage electrode. As a consequence, for exposures lower than the saturation level<sup>\*7</sup>, all the photogenerated holes that diffuse under the sensing electrode end up by being swept to the storage well.

In the second stage of operation (*readout before transfer*), the sensing gate is left floating while its voltage is measured. The sensing gate is the upper electrode of a MOS capacitor in equilibrium, and as a result its potential will remain constant for a while (in time, the dark currents will fill up the potential wells with thermally generated minority carriers). There is however an uncertainty in measuring the preset voltage (-4V in the illustrated example) known as reset noise or KTC noise. The reason for measuring the sensing gate voltage at this stage is to remove the reset noise by correlated double sampling (CDS)<sup>24</sup>. In the third stage, the potential well under the storage electrode is collapsed and all the holes will move to the well under the sensing electrode. As a result, the measured voltage of the sensing gate (which is connected to a high input impedance amplifier, hence floating) will increase by a value proportional to the amount of charge transferred. In CDS readout mode, the voltage readout before transfer and the voltage

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<sup>\*7</sup> A pixel is saturated when the amount of charge exceeds the pixel charge storage capacity and some charge starts spilling over from the storage well to the sensing well, or to neighboring pixels.

after transfer are subtracted, and the value is considered the signal. When properly done, this removes the reset noise from the signal and reduces the effect of low frequency (1/f) noise of the amplifier<sup>32</sup>.

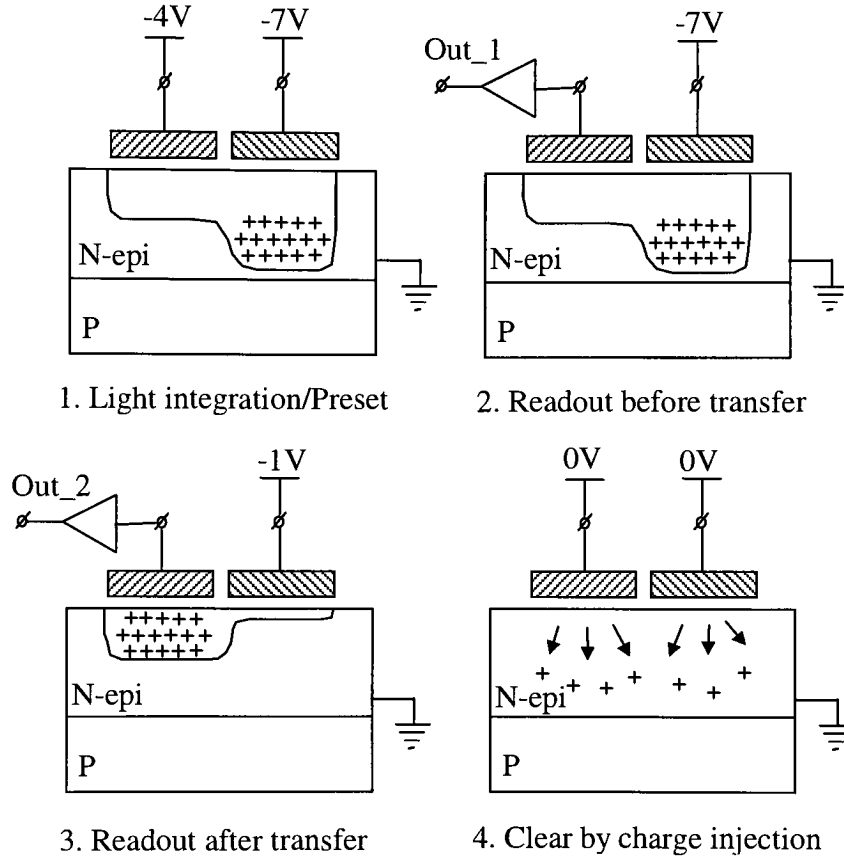


Figure 1.8 Working principle illustration of a two-electrode P-channel CID pixel. The right hand side electrode is the sensing electrode.

By proper manipulation of the electrode voltages, the charge can be transferred back and forth between the storage well and the sensing well. No significant amount of electrical charge is lost during the transfer and non-destructive readout (NDRO)<sup>21</sup> can be performed.

The *inject* operation follows the readout, and now the potential wells are collapsed under both electrodes and the charge diffuses away, being eventually swept into the substrate across the reverse biased P-N junction.

#### ***1.3.2.2. The operation of the three-electrode pixel***

There are two disadvantages in using a two-electrode pixel structure for a CID. The most important comes from the capacitive coupling between the sensing gate and the storage gate. This materializes in a path through which the clocking signal driving the storage gate can couple to the sensing node. This effect is known as *clock feedthrough*. There are ways to compensate for the clocking artifacts in the output signal such as by introducing a clocking component equal and opposite in phase. There is however a fixed pattern noise component and a temporal noise component associated with the clocking signal, which are random and can not be compensated.

Another disadvantage of using a two-electrode structure is the reduced well capacity. In order to function, the storage well has to be about double the size of the sensing well. This condition, in case of equal area electrodes, means that only half of the maximum allowable gate voltage will define the well capacity. This becomes a more serious limitation when deep sub-micron IC processes are used for device fabrication, and where the supply voltage is reduced (e.g. 3V for a 0.35-micron process).

The operation and layout of the three-electrode pixel structure are similar but slightly more complex than the operation and layout of the two-electrode structure. While in integration mode, charge is collected in both sensing and storage potential wells. In the two-electrode structure while in integration, the charge will naturally flow from the sensing to the storage potential well due to the difference of potential depth. In the three-electrode structure, there is the need of an additional phase prior to readout, called *back-*



*transfer*, while the electric charge is transferred from the sensing potential well to the storage potential well after the light integration prior to readout (see Figure 1.9).

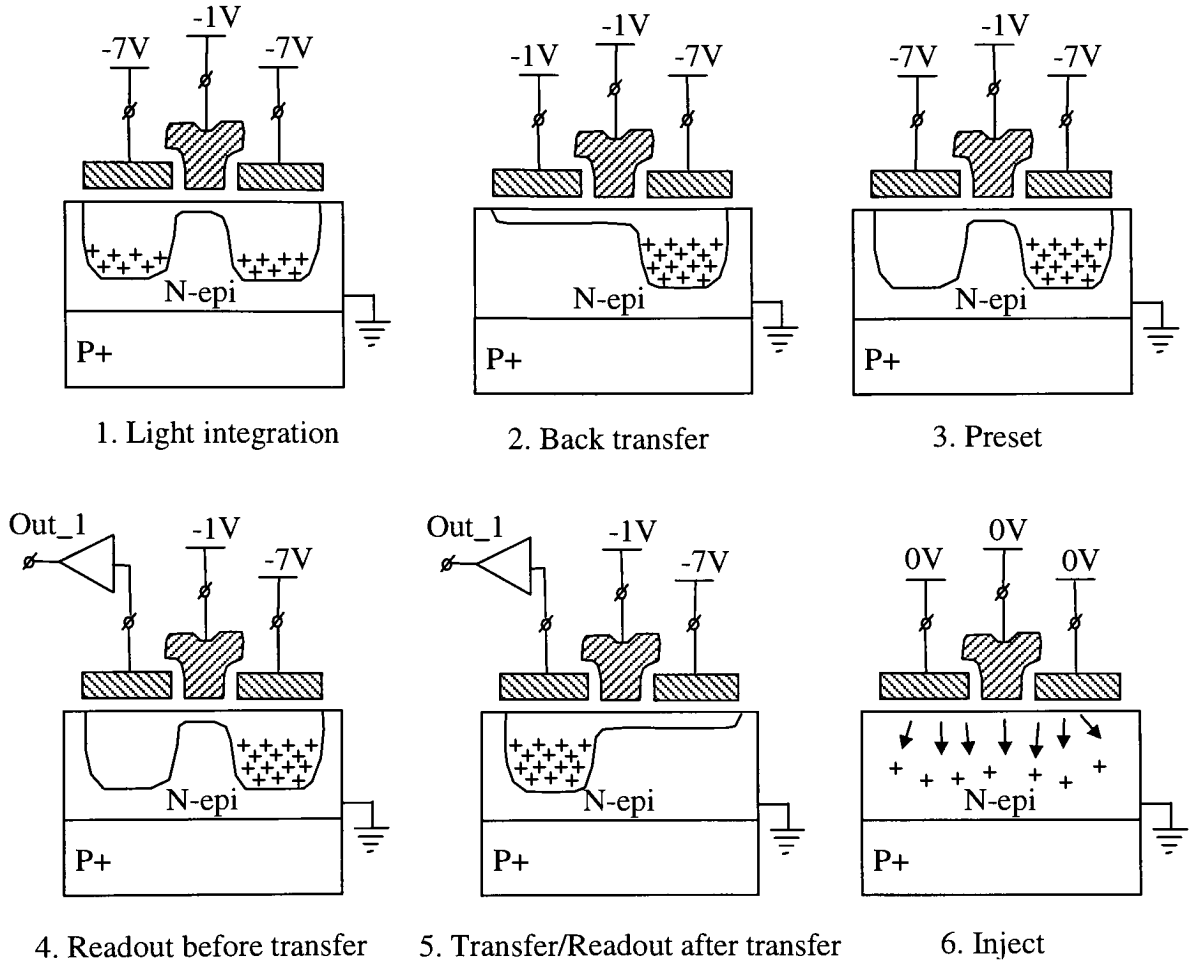


Figure 1.9 Working principle illustration of a three-electrode P-channel CID. From left to right the function of the electrodes are as following: sensing, transfer and storage.

From a layout perspective, a three-electrode structure needs an extra bus for biasing the transfer gate. Although more complex than the two-electrode architecture, the three-electrode structure performs better from a practical standpoint, improving the full well capacity and giving images virtually free from fixed pattern noise in passive CID imagers.

### 1.3.2.3. *The architecture and operation of a CID imager*

An advantage of the CCD, in its early stages of evolution, was the lack of active, on-chip driving electronics. The structure of the electrodes itself led to a self-scanning array. In the case of the CID, this is not true since charge transfer and charge-to-voltage conversion occurs within each pixel [sections 1.3.2.1 and 1.3.2.2]. By connecting all the sensing electrodes of pixels along the rows to row buses and all the storage electrodes along columns to column buses it is possible to randomly select individual pixels or rectangular groups of pixels. The selected pixel(s) can be put in modes of operations different than the rest of the array. To do this it is necessary that each row and each column is provided with active electronic circuitry.

## Column/row scanners

The column/row on-chip drivers are called scanners. The CID imager can be implemented with features such as *random address readout*, *multiple readout*, *random address injection*, *random pixel binning*.

As consequence, the scanners for a scientific CID imager can be quite elaborate<sup>21</sup>. In the generic scanner presented here, the addresses can be loaded into the decoder either directly from the outside or from an on-chip counter. The address decoder activates one line/column at a time and loads a binary “1” into the shift register. The shift register, which is initially reset, can therefore be progressively loaded with binary “1’s”, in random positions. In order to scan the array, after the load operation is finished, the information in the register can be shifted to the left or to the right. A logic “1” in a certain stage of the shift register means that the corresponding rows/columns are being selected.

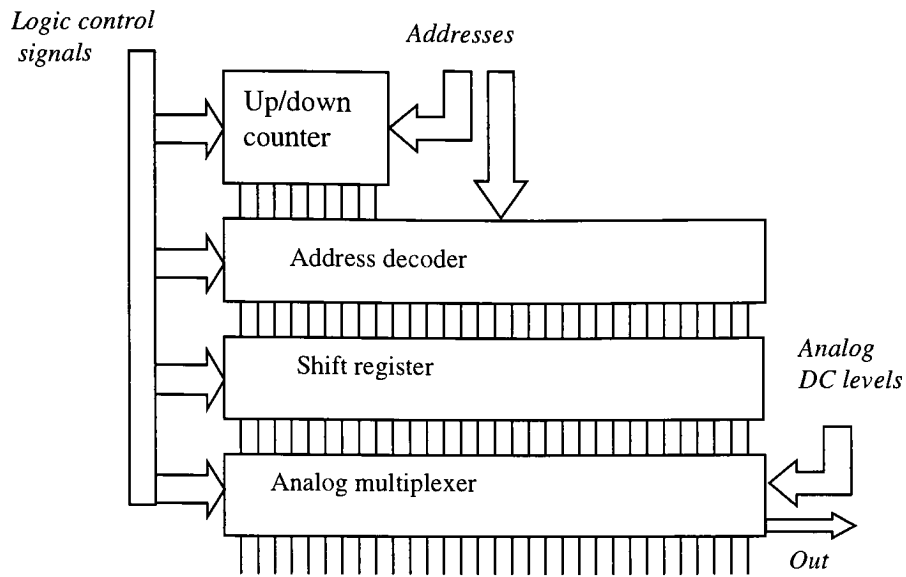


Figure 1.10 Block diagram of a generic CID scanner

Function of the value of the *analog DC levels* (see Figure 1.10) fed into the multiplexer, the selected rows/columns can be driven into injection mode, charge storage mode, or readout mode. In this way, random rectangular regions of the arrays can be *injected*, or can be *readout* simultaneously (pixel binning) while the rest of the array is kept in an *charge storage* mode

## Charge readout

Figure 1.11 illustrate a simplified current flow model during readout of a P-channel CID pixel<sup>22</sup>. Setting the storage electrode at  $-1V$  collapses the corresponding potential well and forces the minority carriers to move under the sensing gate.

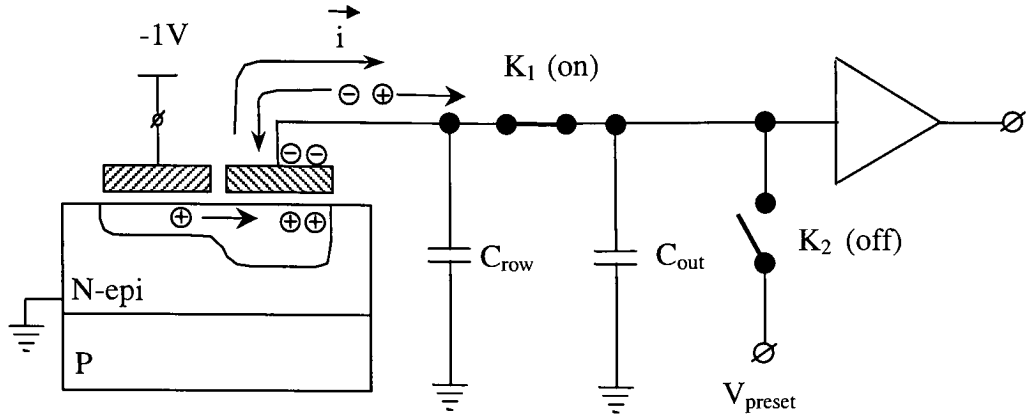


Figure 1.11 CID voltage readout mechanism.

$C_{\text{row}}$  is the capacitance associated with a row (which include the sensing gate capacitance), and  $C_{\text{out}}$  is the capacitance of the output-multiplexed bus, plus the input capacitance of the preamplifier.  $K_1$  is the row selection switch, and  $K_2$  is a preset switch. The current  $i$  integrated in time is equal to the transferred charge.

$$\Delta V = \frac{Q_{\text{transfer}}}{C_{\text{sensing\_node}}} = \frac{Q_{\text{transfer}}}{C_{\text{row}} + C_{\text{out}}} = Q_{\text{transfer}} \cdot \text{Gain} \quad (1.6)$$

A first order approximation of the voltage variation on the input node function of the transferred charge is given by (1.6).

The inverse of the sensing node capacitance is the conversion gain defined as the variation of the voltage while the charge in the potential well varies by one electron (or hole - depending on the type of the substrate). A typical value for the total capacitance is around 20 - 30pF for a passive CID array and can go down to 10 - 15pF for a preamplifier per row (PPR) architecture. As this type of readout can be used in most of the image sensors, it is important to notice that the minimum charge detectable with an amplifier that has a given equivalent noise input voltage, is inversely proportional to the conversion gain. For a CCD, the output node capacitance is typically a fraction of picofarad. The gain

of a CCD will be about two orders of magnitude higher than the gain of a passive CID. Hence the noise performance of a CCD will be much better than that of a CID if both are to be built in similar technologies (with amplifiers having similar noise performance and readout at the same speed). While for a CCD the noise performance is not directly influenced by the size of the array (the charge is carried to the output preamplifier where the charge-voltage conversion occurs), the noise performance of a CID will decrease proportionally with the length of the row (because  $C_{\text{row}}$  increases).

#### ***1.3.2.4. Advantages of the CID imager***

***Random pixel addressing:*** The pixels of a CID array can be readout in any order. This enables more efficient modes of extracting the information from the image.

***Nondestructive/multiple readout:*** CID pixels can be readout nondestructively, multiple times, without losing photo-charge. This allows charge monitoring during integration and readout noise reduction techniques.

***Radiation tolerance:*** Most of the CID imagers are built as all PMOS structures that are inherently radiation tolerant. The threshold shifts down in value while increasing exposure to radiation i.e. an increase in the absolute threshold value for a PMOS structure. Adjusting bias voltages can compensate for the threshold shift while maintaining functionality. Degradation in charge transfer efficiency is not an issue here because the electric charge is transferred along short distances, within the pixel only.

***Reduced sensitivity to point defects:*** Because of the lack of inter-pixel charge transfer, any physical damage to the sensing area doesn't affect the charge transfer/sensing process in the neighboring pixels. The effect of a point defect will remain localized to a certain pixel.

***Inherent anti-blooming properties:*** The CID imager is built on an epitaxial layer, which forms with the substrate a reverse biased vertical PN junction. If the photo-generated

carrier number exceeds the pixel capacity, the excess of charge will be swept to the substrate by the built-in potential of the vertical PN junction. The thickness of the substrate establishes a tradeoff between the light sensitivity and modulation transfer function (MTF) (blooming can be regarded as a severe degradation of the MTF at high light levels).

***Contiguous pixels:*** The pixels are separated by field oxide, which makes the border between pixels, light sensitive. The contiguous CID pixel structure lends itself to a high degree of sub-pixel interpolation<sup>23</sup>.

***Good quantum efficiency in blue and UV light:*** The large unobstructed silicon area of a scientific CID imager pixel can lead to good quantum efficiency for short wavelengths.

***Random pixel binning:*** Random groups of pixels can be readout at the same time. The output is proportional to the integrated electric charge contained in the selected group of pixels.

***Easy to implement in a standard CMOS process:*** As opposed to the CCD, which requires a very special process, the CID can be fabricated in a standard CMOS process with few modifications. This allows the designer to place various electronic blocks on the same chip with the imager.

#### ***1.3.2.5. Limitations of the CID imager***

***Large readout noise:*** All the sensing gates along the row of a passive pixel CID imager are connected in parallel, resulting in a high parasitic capacitance of the readout bus, hence a lower gain and lower overall noise performance (section 1.3.2.3 – Charge readout).

***Low dynamic range:*** A high noise determines a high dynamic range, which is defined as the full well capacity divided by the readout noise.

***Crosstalk:*** There are several crosstalk mechanisms described in literature<sup>19</sup>. Most have to do with the column-row crossover capacitance.

## 1.4. The (passive pixel) XY-addressable imaging array

In general any array that has one or more MOS or bipolar-junction transistor(s) (BJT)<sup>15</sup> used as switches, but not as a preamplifier, in each pixel, can be included in this category. There is a wide selection in choosing the photosensitive element. Monolithic as well as hybrid implementations are available. However because the most common choice is the photodiode, this particular type of array will be further presented.

### 1.4.1. The architecture of the passive pixel photodiode array

The simplest form of photodiode array, given as a generic example, contains a photodiode and one MOS transistor in each pixel.

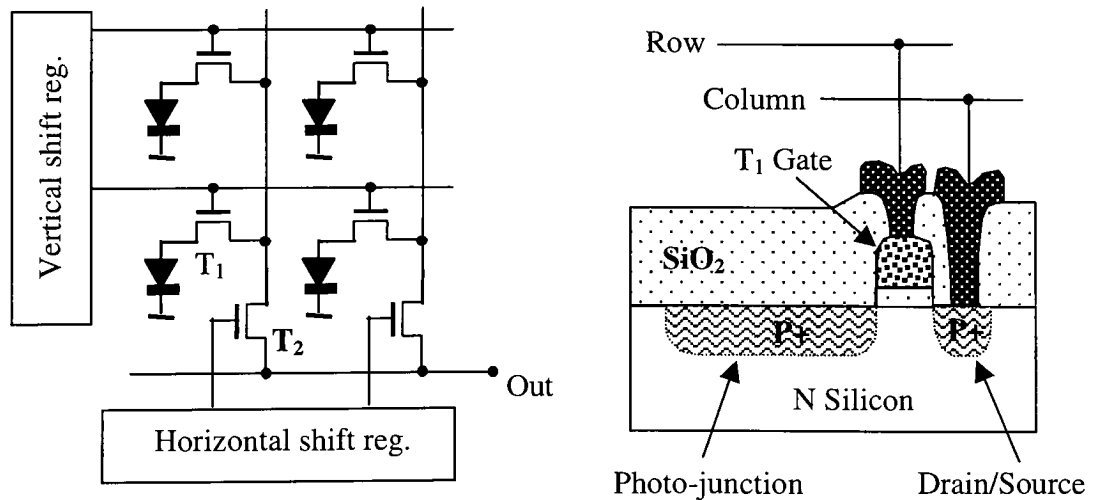


Figure 1.12 A block of two-by-two pixels for a passive-pixel MOS XY-addressable photodiode imaging array (a), and a generic pixel section (b)



The transistors are used as switches, having the gates connected together along the row, and one of the source terminals connected along the column. The drain terminal represents the anode of the photodiode. The substrate is the common cathode for all the photodiodes in the array.

A two-by-two pixel block of a photodiode array is shown in Figure 1.12. In this particular example the device handles electrons as photo-generated charge.

### **1.4.2. The working principle of the passive pixel photodiode array**

As the working principle is concerned, the photodiode has to initially be preset at a certain positive voltage,  $V_{preset}$  (reverse bias the photo-junction). Then the junction is left floating during the light exposure. The preset phase is done again by turning on both transistors ( $T_1$  and  $T_2$  in Figure 1.12), which connect the cathode of the junction to the output of the array, and setting the output terminal to  $V_{preset}$ . This operation is done during the phase of readout while the integrated charge necessary to preset the photodiode (and which is equal to the photo-generated charge) is sequentially measured for each pixel (current readout). This means the readout of one row within a frame is done at the same time as the preset operation but for the next frame.

### **1.4.3. Advantages of the passive pixel photodiode array imager**

The advantages of this type of imager are: random pixel addressing, high quantum efficiency in blue light, insensitivity to point defects, possibility to do random pixel binning, high well capacity, and the ease to implement the present architecture in a CMOS process.

#### **1.4.4. Limitations of the passive pixel photodiode array**

The limitations of this type of imager are destructive readout and high readout noise. The high noise level is due to the large input node capacitance added to the fact that the correlated double sampling readout technique cannot be properly applied to this type of imager. Unlike the CID, the photodiode array has no intra-pixel charge transfer and only one output value is available for each pixel readout (during the preset). Therefore it is not possible to cancel out the reset (KTC) noise of the photodiode (see section 1.3.2.1). Another disadvantage to mention for any passive pixel XY-addressable imaging array is the pixel crosstalk which means the output signal read from one pixel is dependent on the photo-charge existent in other pixels of the array.

## 1.5. The active pixel imaging array

The active pixel concept signifies the existence of at least an active component (signal preamplifier) in each pixel. Besides the photosensitive element (CCD, CID, photodiode, etc), the pixel typically contains three to four MOS transistors (the preamplifier and 2-3 switches). The signal to noise ratio of this structure is expected to improve considerably compared to the passive version.

### 1.5.1. The architecture of an active pixel imaging array

Figure 1.13 represents the generic schematic of a 2x2 active pixel photodiode array in the active pixel version.

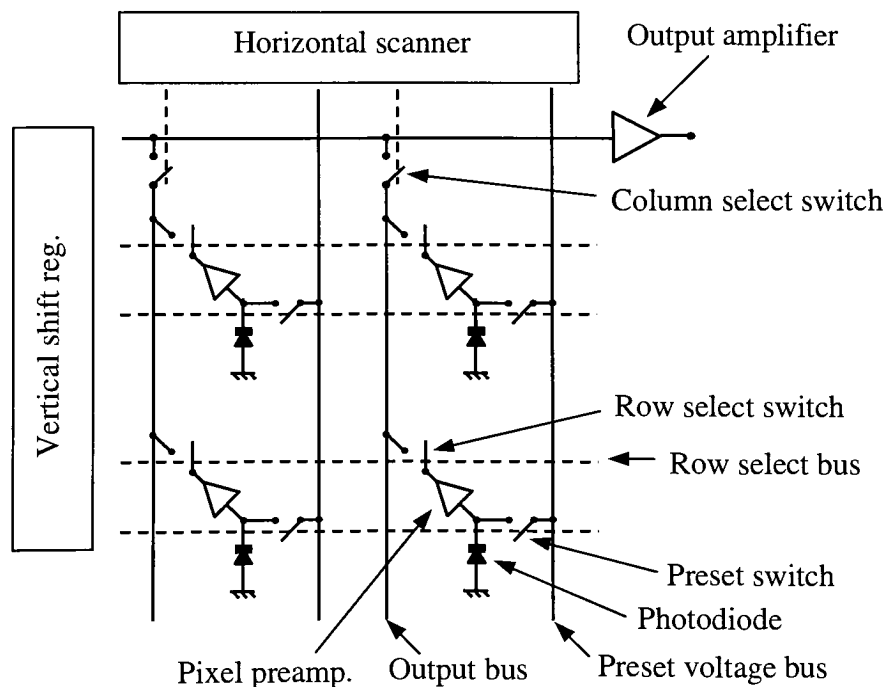


Figure 1.13 The schematic of an active pixel photodiode imaging array.

There are possible various readout modes, each of which would lead to a particular array architecture.

### 1.5.2. The working principle of the active pixel photodiode imaging array

**Preset:** For the particular array depicted in Figure 1.13, all the photodiodes are simultaneously set to a reverse biased condition by closing the preset switches in all the pixels of the array.

**Light integration:** All the preset switches are opened and the photodiodes are left floating for a certain period of time while the array is illuminated by the scene. If the light exposure is zero, and the integration time is small (negligible dark current effects), the photodiodes are supposed to maintain their potential constant. For nonzero light exposure, the built-in electrical field sweeps the photo-generated minority carriers generated in vicinity of the PN junction across the junction. Because the PN junction acts similarly to a charged capacitor<sup>24</sup>, the electrical potential difference across the photodiode will decrease proportionally to the amount of charge crossing the junction.

**Readout:** In this example a *fast-horizontal* readout mode is presented. In each pixel, the difference between the preset voltage and the voltage across the photo-junction after the exposure will be proportional to the light exposure of that pixel. The preamplifier is typically a buffer with a near-unity voltage gain. All the row select switches for the first row are closed during the readout of this row. The column select switches are then closed, one at a time, in a serial fashion. The voltage information for all the photo-junctions in the first row is serially transferred to the output. One by one, the rest of the rows are read in the same way.

### 1.5.3. Advantages and limitations of the active pixel imaging array

Depending on the photosensitive element (photodiode, CCD, CID, photoresistor, etc) the advantages and limitations of the active pixel imagers may vary. There are however two distinct advantages in building an active pixel. These are as *better noise performance* and *crosstalk protection*. Placing an amplifier in the pixel the *complexity of the pixel layout increases* while *fill factor* (hence *quantum efficiency*) decreases. Another drawback is a *significantly higher fixed pattern noise* (which results from the dispersion of the pixel preamplifier parameters).

## 1.6. Noise in imaging arrays

While imaging a static scene, the output of any pixel in a given imager is supposed to be constant from frame to frame. In reality, variations about the mean-level values always occur due to the presence of noise. Noise is a statistical process and it manifests itself as random fluctuations in the imager output while the scene is constant. It is usually characterized by the root mean square (r.m.s.) variation of the instantaneous signal level  $S_i$ .

$$N_{r.m.s.} = \sqrt{\frac{\sum_{i=1}^n (S_i - S_{average})^2}{n}} \quad (1.7)$$

where  $S_i$  is the mean signal level and  $n$  is the number of samples. To make noise a more meaningful parameter it is useful to be defined relative to some average or maximum average signal and in this case a new parameter is defined, the signal-to-noise ratio ( $S/N$ ).

Noise is added in every stage of the imaging chain starting with the image itself. If the noise sources are uncorrelated, then they simply add in quadrature such that:

$$N_{sum} = \sqrt{N_1^2 + N_2^2} \quad (1.8)$$

Due to the nature of the quadrature addition, the larger the noise source, the more dominant effect will have in the final image. This is important to know when applying noise reduction techniques because targeting the largest noise source will have the largest effect in the final image.

There are several different noise sources that affect a solid-state imaging chain as presented in the diagram below.

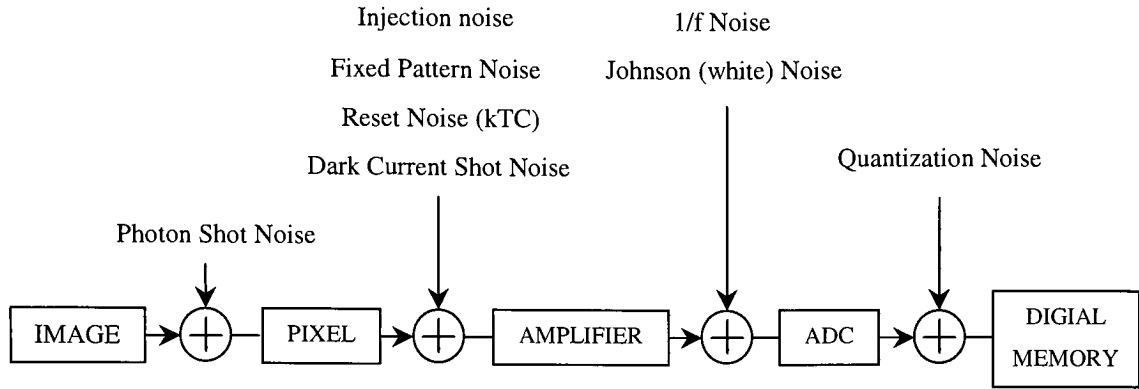


Figure 1.14 Noise sources in a solid state imaging chain

### 1.6.1. Photon shot noise

Shot noise is a fundamental type of noise that arises from counting statistics. A flow of electrons or photons, rather than being continuous, is composed of a stream of discrete particles. The process of estimating the number of particles passing through a certain surface in a certain time is governed by a Poisson statistics. The error  $\sigma$  (standard deviation) of determining an average number of particles  $N$  is determined by:

$$\sigma = \sqrt{N} \quad (1.9)$$

In our case we can see that there is an intrinsic noise associated with the image itself and which is not dependent on the imaging system employed.

There is a signal-to-noise ratio in any image and which is better for brighter images. Ideally the imaging chain has to be designed so that the signal-to-noise ratio is unaffected by the imaging chain.

$$\frac{S}{N} = \sqrt{N} \quad (1.10)$$

Looking at (1.9) it is easy to see that there is always a low enough light level below which the imaging chain noise will exceed the scene noise.

### 1.6.2. Dark current shot noise

Dark current occurs due to the thermal generation of free minority carriers around defects within the semiconductor bulk or at the semiconductor-oxide interface. Having typical values around hundreds of pA/cm<sup>2</sup> for surface channel devices, at room temperature, the value of the dark current doubles for every 8 K increase in temperature<sup>24</sup>.

The effects of the average dark current can be compensated by always reading a dark reference pixel and subtracting this value from the output value of the normal image pixel. The problem is that dark current obeys a Poisson statistics and it has a shot noise associated with it. The value of this noise is equal to the square root of the dark current generated charge (expressed in electrons). This shot noise associated with the dark current cannot be compensated. Trying to compensate for the average of the dark current by the method described above will actually increase the noise at the output since now there the noise from reading two pixels (image pixel and dark pixel) will add in quadrature.

The easiest way to avoid the dark current shot noise is to cool the device down to a temperature where the dark current shot noise is small compared to the rest of the imager noise.

In certain cases especially where there the light intensity is high there is the option of running the imager very fast so that the dark current and dark current shot noise are minimized.



### 1.6.3. Reset (kTC) noise

The reset noise (also called KTC noise) is due to the uncertainty a capacitor (in our case the sensing MOS capacitor) can be charged at a given voltage through a resistor. This uncertainty is induced by the thermal noise across the resistor and it depends only on the value of the capacitance and temperature<sup>25</sup> by the following relationship:

$$\Delta n = \frac{1}{q} \sqrt{kTC} = 400 \sqrt{C[pF]}_{room\_temperature} \quad (1.11)$$

where  $k$  is Boltzman's constant,  $T$  is the absolute temperature,  $C$  is the capacitance expressed in picofarads and  $\Delta n$  is the reset noise in electrons. This will correspond to 40 electrons r.m.s. reset noise for a 10fF capacitor at 300K. At liquid nitrogen temperature (77K) this value is halved. Using the CDS readout technique the reset noise can be efficiently suppressed<sup>25</sup>.

### 1.6.4. Fixed pattern noise (FPN)

Generally speaking, FPN of an imaging array represents the pixel-to-pixel variation in output signal under uniform illumination. The image of an arbitrary scene and the fixed pattern noise will overlap at the output of the imager. Visually one has the impression of viewing the scene through a stained glass. This is a serious drawback especially in active pixel sensors, and is mainly caused by pixel to pixel variations in the pixel parameters. While the previous types of noise can be classified as "temporal noise", FPN is a "spatial noise".

The FPN can be corrected to a certain extent. On-chip solutions are usually cheap but not so effective. CDS readout partly corrects this problem. Off chip solutions require

computation power but they can be really effective. Such FPN reduction techniques will be analyzed in section 4.4.1.

### 1.6.5. Injection noise

The CID device described here is a surface channel device. This means that the photogenerated electrical charge (electrons) is stored under the electrodes, in the silicon at the interface with the oxide. The charge transfer between the capacitors also occurs next to the surface. The silicon-oxide interface has defects inducing a trapping-and-releasing effect on the electric charge carriers, hence generating noise<sup>25,26</sup>. In order to maximize transfer efficiency and reduce the transfer noise, the interface traps have to be kept filled with electrons at any given time by keeping a small amount of charge (fat-zero<sup>28,27</sup>) in the potential wells.

It is hard to assess the state of the surface in a given process and the amount of fat-zero needed to obtain linear transfer characteristics. However a rough estimation of hundreds to thousand of charge carriers is a reasonable value. The shot noise associated with this charge assuming a Poisson statistic must be in the order of few tens of electrons.

Two of the main components of the injection noise, the kTC injection noise and the injection shot noise are introduced below.

#### *1.6.5.1. Electrical fat-zero – KTC injection noise*

In this situation a minimum depth potential well has to be maintained under each photogate during injection. The MOS capacitors have to be kept in an inversion state (the voltage on the photogates larger in absolute value than the threshold voltage).

There is a threshold voltage variation across the imager due to the manufacturing process. The state of the art technologies were able to reduce this variation below several millivolts over large surfaces. In order to make sure the surface states are not depleted in any of the MOS capacitors corresponding to the photogates, the injection operation has to be done at a voltage slightly lower than the threshold voltage.

Due to the threshold voltage nonuniformity the residual charge left in each potential well is different from pixel to pixel. Even for the same capacitor this charge is different after each injection operation due to the uncertainty the sensing and storage buses are set at the inject-level voltage (KTC noise).

#### ***1.6.5.2. Optical fat zero – injection shot noise***

A different injection technique inspired by the operation of the surface channel CCD can be used for injection. In this case, a harder initial injection is done, by setting the photogates at potentials under the threshold voltage. Part of the surface states will be depleted. Then, an optical fat-zero charge is introduced by shortly exposing the array to a uniform optical radiation.

The fat-zero generation mechanism is described by a Poisson statistics<sup>28</sup>. The associated noise will be given by the square root of the quantity of charge introduced which is characteristic to a shot-noise limited process.

### **1.6.6. The preamplifier noise**

A MOS transistor in source follower configuration is used as a preamplifier. The preamplifier introduces two main noise components: the thermal white (Johnson) noise and the flicker (1/f) noise<sup>29,30</sup>. Depending how fast the readout takes place one noise

source tends to dominate the other. Typically at tens of kilohertz where the arrays described here are operated the 1/f noise is the dominating component in the preamplifier noise.

#### **1.6.6.1. Johnson noise**

Johnson (thermal/white) noise in resistors is due to the random thermal motion of electrons and unaffected by the presence or absence of direct current. In a resistor the voltage variance due to this type of noise is<sup>29</sup>:

$$\overline{v}_{resistor}^2 = 4kTR\Delta f \quad (1.12)$$

In a MOS transistor the formula becomes:

$$\overline{v}_{Johnson\_FET}^2 = \frac{4 \cdot k \cdot T \cdot \Delta f}{g_m} \quad (1.13)$$

where k is Boltzman's constant, T is the absolute temperature, R is the resistance and  $g_m$  is the transconductance of a field effect MOS transistor<sup>29</sup>. Since  $g_m$  is given by:

$$g_m = \sqrt{2I_{sat} \cdot \beta} \quad (1.14)$$

$$\beta = \frac{\mu_p \cdot \epsilon}{t_{ox}} \cdot \frac{W}{L} \quad (1.15)$$

$I_{sat}$  is the value of the DC current through the transistor at saturation

$\mu_p$  is the hole mobility and it is a material constant (typically 200 cm<sup>2</sup>/V\*sec)

- $\epsilon$  is the absolute electric permittivity of silicon
- $t_{ox}$  is the thickness of the gate oxide
- $W/L$  is the ratio width over length for the gate of the MOS transistor under study

The preamplifier transistor used in these imagers works in saturation regime, under constant current as a source follower. From the above formulas we can see that in order to minimize the Johnson noise, some parameters can be acted upon such as:

- $T$  is the temperature and has to be decreased. Even large CID arrays can work well at liquid nitrogen temperature (77K) since charge transfer efficiency is not such a problem as in CCD's.
- $\Delta f$  is the frequency bandwidth. It has to be restricted as much as possible by using low pass filter within the amplification chain.
- $I_{sat}$  is the DC bias current and it can be increased as much as the increase in chip power consumption is tolerable. There is also an electrical constraint for the maximum value of this current dictated by the dynamic range, the gain and the linearity of the source follower preamplifier.
- $t_{ox}$  is the thickness of the gate oxide. The thinner the oxide the better. This is a process constant and it cannot be changed but by changing the process.
- $W/L$  the width over length ratio of the gate transistor. This can be increased within certain limits dictated by geometrical constraints and design rules.

#### **1.6.6.2. Flicker (1/f) noise**

1/f noise has been observed in all kind of devices, from homogenous metal film resistors to different kinds of semiconductor devices. It is due to bulk or surface traps, which interfere with the conduction mechanism. Because 1/f noise is wide spread over

different types of electronic components people think there is a fundamental physics mechanism behind it. Till now such a mechanism has not yet been found<sup>31</sup>.

The MOS transistor has the highest 1/f noise of all active semiconductor devices due to its surface conduction mechanism. There are several models describing this type of noise one of which being the mobility fluctuation model<sup>31</sup> developed by Hooge.

Based on this model, the voltage variance in a MOS transistor can be expressed as:

$$\overline{v_{1/f}^2} = \text{const} \tan t \cdot \frac{t_{ox} \cdot (V_{GS} - V_T)}{W \cdot L \cdot f} \quad (1.16)$$

From the above formula we can see that in order to minimize the Johnson noise, some parameters can be acted upon such as:

- $t_{ox}$  is the thickness of the gate oxide. The thinner the oxide the better. This is a process constant and it cannot be changed but by changing the process.
- $W \cdot L$  is the gate area (the larger the better).

### 1.6.7. Quantization noise

The process of converting a continuous analog signal into a set of discrete levels is called quantization. The quantization noise is the inherent uncertainty introduced during quantization since only discrete, rather than continuous levels are generated. Also called quantization distortion. This noise can be made negligible by selecting the quantization step to be several times smaller than the noise of the imager referred at the input of the A/D converter.

In our case, using a 16-bit A/D converter with the input range between 0V and 10V, the quantization step is 152  $\mu$ V. Since the dynamic range for 388x16 Orbit AP-CID

is expected to be well below 100,000, a gain bringing the maximum output signal of the imager close to 10V is satisfactory. For safety all the mean variance (noise measurement) tests were done with about three times that gain.

This means that for the noise measurement the imager was always kept in the lower region (less than 25%) of the dynamic range in order to avoid the saturation of the A/D converter. To confirm the above assumptions, the noise of the imager for that gain was measured in the range of 10-12 ADU (analog to digital units). The noise with the imager output grounded was around 4 ADU. This included the off chip amplifier chain noise, CDS noise and quantization noise.

### **1.6.8. Noise balance**

Spot noise measurements done at CIDTEC on P-channel MOS transistors were used to estimate the noise parameters of the preamplifier transistor. To find and plot the output noise power spectrum of the preamplifier a *Mathcad* calculation was done (example in Appendix)

In order to suppress the reset noise and reduce the  $1/f$  noise, the output of the preamplifier is passed through a low pass filter followed by a CDS block. The output power spectrum is calculated in the same appendix based on results published by Pimbley and Michon<sup>32</sup>.

The integrated noise power spectrum gives the preamplifier readout noise, which is expected to be several electrons r.m.s. at a temperature of 250K and 20kHz pixel readout rate.

If CDS readout is used, the main contributing components to the readout noise are the injection noise and the preamplifier noise. The two sources of noise are uncorrelated hence they will add in quadrature. The main component in the noise balance is expected to be the injection noise (section 1.6.5).

## Chapter 2. The low-noise AP-CID imager

In this chapter the basic concept of AP-CID is introduced. Different architectures and modes of operation are analyzed. Several structures, which have been fabricated and tested, are presented. The development of this type of sensor took several years to accomplish. The most advanced array (Orbit 388x16) was measured at less than 10-electron readout noise at minus 30°C temperature. This is in the range of scientific CCD performance and about 2 orders of magnitude better temporal noise performance than traditional CID's. These are the first active pixel CID imagers in existence.

### 2.1. Array review

Four different arrays were fabricated. Table 2.1 contains a summary of the characteristics of these arrays.

The first array in the list, the 8x8 RIT AP-CID was designed by Dr. Gerrit Lubberts and Zoran Uskocovic in 1997. A working version of this array was also fabricated and tested by the author together with Gerrit Lubberts at RIT in the spring of 1998. This was a feasibility study trying to assess the possibility to fabricate CID devices in the local foundry. The array was driven by off-chip scanners and was using 2-electrode pixels. The temporal noise and fixed pattern noise of this array were high (about 1500 electrons for the temporal noise). The clock feedthrough was also larger than the signal which prompted the designers to consider means of cancellation (1.3.2.2).

The second array, the 54x40 RIT AP-CID was designed and fabricated by George Lungu and Dr. Gerrit Lubberts. This array was a more elaborate design having on chip scanners and three electrodes per pixels. Even though the imager was functional the very



	Mini- mum feature size	Pixel size	Design fill factor	Proces s	Transfer gate/ Readout	Remarks
8x8 RIT AP-CID	6 $\mu$ m	200 $\mu$ m	6%	PMOS	No/Fast vertical	Feasibility study/ off chip scanners
54x40 RIT AP-CID	6 $\mu$ m	90 $\mu$ m	35%	PMOS	Yes/Fast vertical	On chip scanners/ fast vertical
128x128 Orbit AP-CID	2 $\mu$ m	41 $\mu$ m	*	CMOS N-well	No/Fast vertical	On chip scanners/ fast vertical
32x32 Mosis AP-CID	0.35 $\mu$ m	11 $\mu$ m	*	CMOS P-well	Yes/Fast horizontal	Not successfully fabricated
388x16 Orbit AP-CID	1.2 $\mu$ m	27 $\mu$ m	*	PMOS	Yes/Fast vertical	8 different pixel types. Good ex- perimental results

Table 2.1 A short summary of the active pixel CID arrays described in this thesis. The first two numbers in the array name indicate its size. The asterisk means that the *design fill factor* (explanation in section 2.3)

large threshold voltage variation across the wafer and across the chip itself rendered it useless for measurements. Both these arrays were built in a PMOS technology, which means that all the MOS structures on the chip were P-channel.

The experience gained developing the first two arrays was used in designing the 128x128 Orbit AP-CID. This device was manufactured in a commercial foundry in a 2 $\mu$ m CMOS process. The pixel has a two-electrode structure. Again, the design proved to be partially functional (the preset operation couldn't be performed) but the performance was not satisfactory for two reasons. The first had to do with the fact that the chip was placed at the periphery of the wafer so the yield and fixed pattern noise were poor (only one working device was found from 9 tested). Also the bond pads were unprotected so that it is possible the devices were electrostatically damaged during the packaging operation.



Figure 2.1 The first images taken with the 128 x 128 AP-CID camera.

No error in the layout was found other than missing bondpad protection. Two images taken with this chip can be found on top of the next page. The third array (32x32 Mosis AP-CID) contained six different imagers having different pixel configurations. It was built in a modern 0.35mm CMOS technology. The purpose of this chip was to study the suitability of deep submicron processes for building AP-CID arrays. (where the design was done). A design error was made which was not detected by the design rule checker.

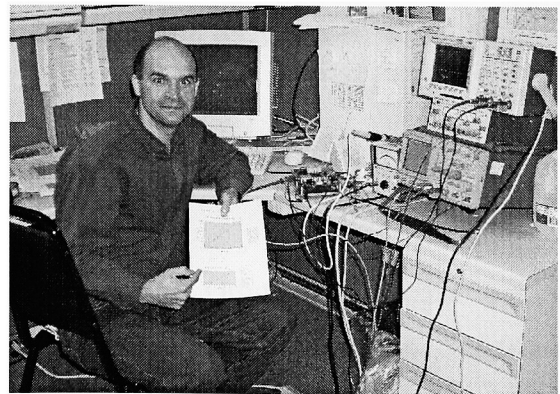
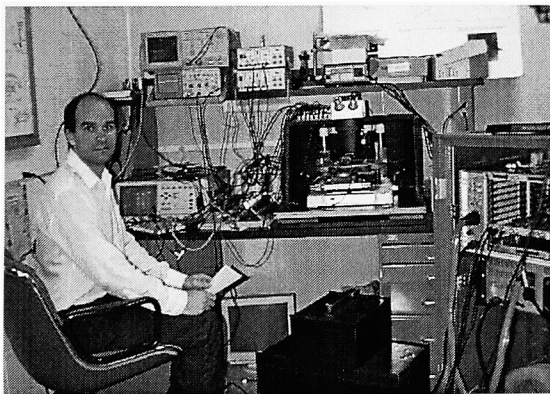


Figure 2.2 Testing sites at RIT and CIDTEC respectively

This array was fabricated but it was not functional. The author designed this chip in a process (MOSIS TSMC 0.35 $\mu$ m) which was not supported on the CAD software at Thermo-CIDTEC. The first photograph above below was taken at the testing site at RIT (testing the 8x8 RIT array at the solid state lab in 1998). The second picture was taken at Thermo-CIDTEC just minutes after obtaining the first mean-variance plot for 388x16 AP-CID array, and which indicated a very low noise count.

Figure 2.3 shows photographs of the first three of the fabricated arrays. The upper three pictures represent large areas of each array while in the lower pictures show individual pixels.

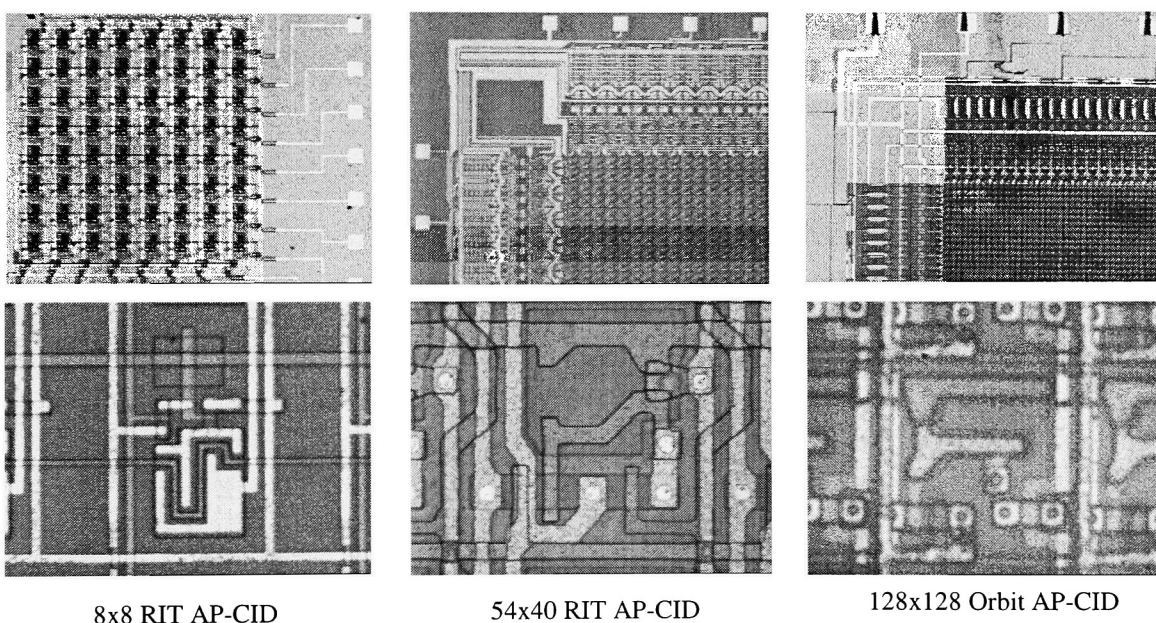


Figure 2.3 Photomicrographs of the first three arrays

The most important chip however is the 388x16 Orbit AP-CID. The author designed and tested this array entirely at Thermo-CIDTEC. The company fully supported the fabrication of this array and partially supported its design and testing. Most of the results and conclusions on AP-CID in this work were based on this array. An important observation to mention here is that the pixels were purposely placed in an N-well where

the concentration of the donor impurities is few orders of magnitude higher than in the native epitaxial silicon (where the pixels of any passive CID array built).

Due to this fact the minority carrier lifetime hence the diffusion length are reduced. Also the depletion regions under the photogates are significantly shallower. All these effects seriously affected the quantum efficiency of this array, which is about an order of magnitude less than expected. It is very important to mention that the rest of the performance was not affected by this decision. The research results and conclusions in this dissertation are valid.

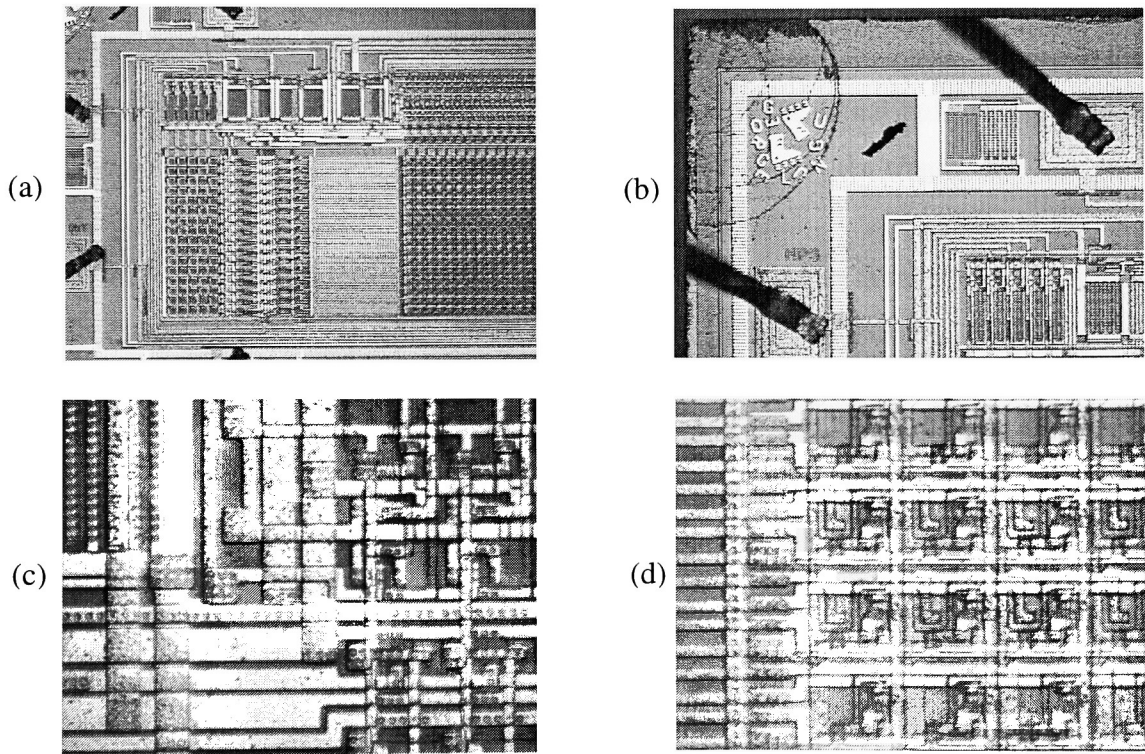


Figure 2.4 Photomicrographs of 388x16 Orbit AP-CID chip

The author unilaterally took the decision to place the whole pixel in the N-well, since at that time an active pixel process had not been developed at CIDTEC. In order to

perform at specified parameters (or just to work) the three transistors in the pixel **have** to be placed in the N-well.

For good quantum efficiency, the N-well could have been masked in the photogate area but for safety reasons all the pixel was built in the well.

Various regions of the 388x16 Orbit AP-CID chip are photographed and presented in Figure 2.4. All the pictures are rotated at 90 degrees for convenience.

The first picture shows a large region of the array. The horizontal scanner is fully visible. Part of the vertical scanner and part of the pixel array are visible also in this picture.

The second picture of the group shows the corner of the array. Two bonding pads with the electrostatic protection circuitry are visible. Two gold wires are connected to the pads. In the lower right corner of this picture there are input signal buffers and analog multiplexers. In the upper left corner there is a designer logo in the shape of two in-line skating shoes.

The third picture shows a zoomed-in portion of the horizontal scanner. The fourth picture shows a zoomed-in region of the pixel array (pixels #5, #6 and #7).

## 2.2. Array architectures

### 2.2.1. General

There are essentially two types of architectures for the active pixel imagers described in this thesis. Both of them use correlated double sampling as readout method. The difference consists in the way the storage electrodes are connected which leads to different readout modes. In the case of the first architecture (8x8, 54x40, 128x128 and 388x16) the storage bus runs horizontally.

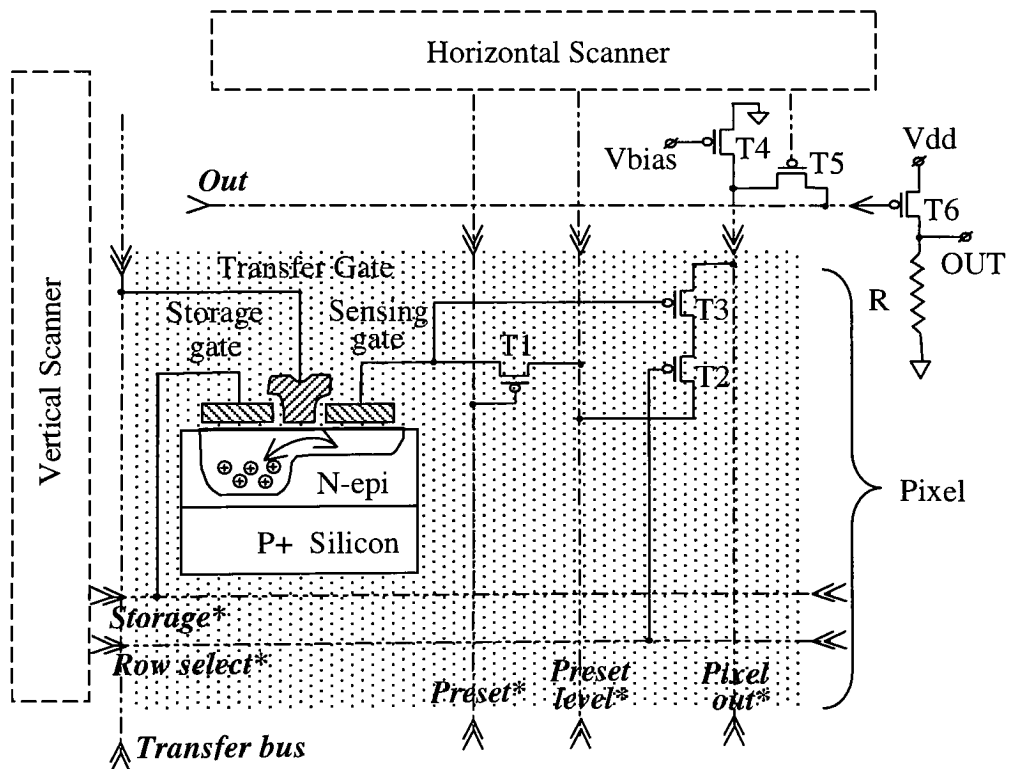


Figure 2.5 Readout schematic for the AP-CID arrays built in fast vertical readout architecture. The pixel schematic is highlighted.

Because the vertical scanner is operated at a higher speed than the horizontal scanner, this is called a *fast-vertical* readout structure.

The schematics of the pixel and the readout chain for the AP-CID arrays in fast-vertical readout architecture are presented in Figure 2.5. Here a three-electrode pixel structure is represented. However, this architecture can equally be used with a two-electrode pixel configuration by eliminating the transfer gate and the corresponding bus.

All MOS transistors represented are P-channel. Transistors T1, T2 and T3 are found in each pixel, whereas transistors T4 and T5 are located at the end of each column. Transistor T1 (*preset transistor*), while on, fixes the sensing gate at the potential of the “*preset level*” bus. Transistor T2 (*row-select transistor*), while on, allows the proper bias of the *preamplifier transistor* (T3) to take place. The gates of all the row-select transistors in a row are coupled together through a *row select bus*. When selecting a certain row, all the preamplifiers in that row are properly biased while all the other rows have unbiased preamplifiers. This way only one of the preamplifiers in the selected row could be coupled to the output while the proper column selection is done. Transistor T3 being part of a source follower preamplifier is coupled to an active load (T4). T4 is part of the column scanner and in the case of 388x16 Orbit array it is placed off chip (common for all columns). The voltage  $V_{\text{bias}}$  sets the current through all the active load transistors, and can be adjusted externally in order to get the best *speed/dynamic-range/linearity* tradeoff. Transistor T5 has a *column-select* function. Transistor T6 coupled to the off-chip resistor R is a source follower amplifier.

The schematics of the pixel and the readout chain for the AP-CID arrays in a fast-horizontal readout architecture are presented in Figure 2.6. The Mosis 32x32 chip is designed in this architecture. Even though this chip hasn’t been successfully fabricated, the concept behind its design is interesting.

There is good similarity between the fast horizontal and fast vertical architectures. To convert from fast vertical to fast horizontal architecture, one has to rotate three buses.

The *storage* bus will now run along the column instead of row, while the *preset* and *preset-level* buses become row buses instead of column buses.

This architecture offers a much faster readout rate due to the fact that while reading a certain row, all the preamplifiers on that row are biased for the whole row readout time.

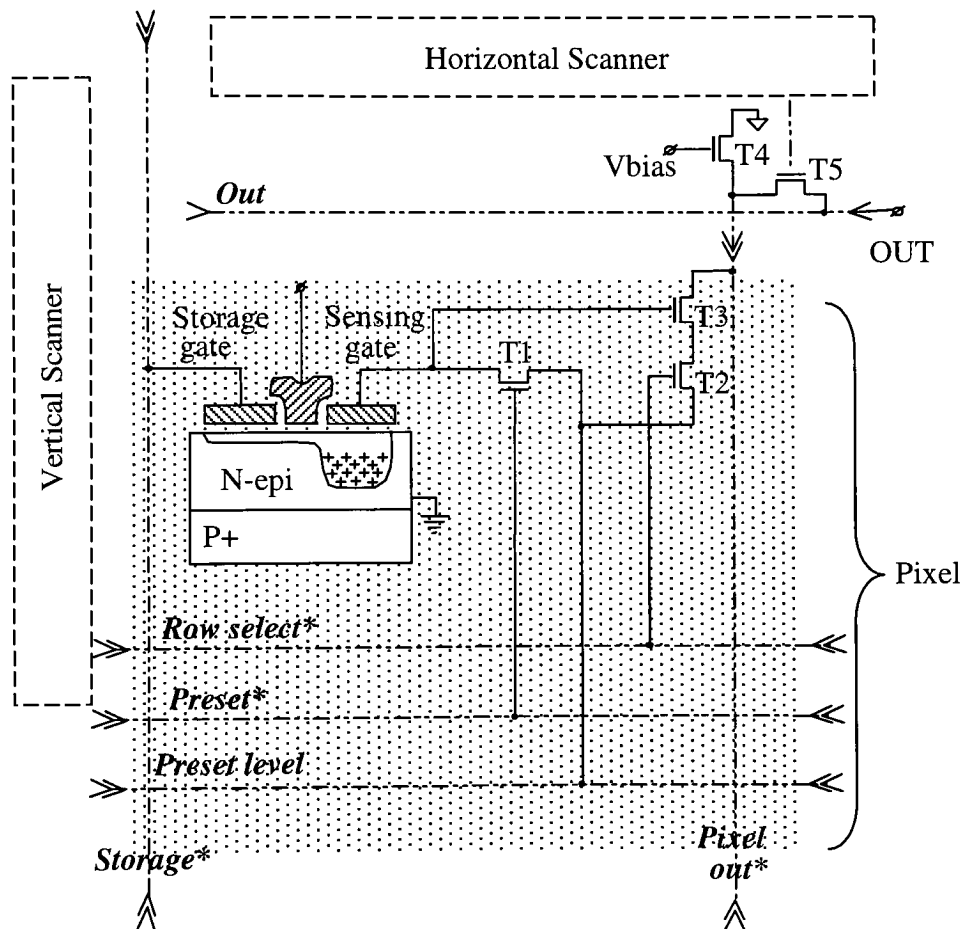


Figure 2.6 Readout schematic for the AP-CID arrays built in fast horizontal readout architecture (MOSIS 32x32). The pixel schematic is highlighted.



No bias current settling time is required for the amplifiers while fast column selection occurs.

An observation worth mentioning is that even though the scanners are fully CMOS, all the transistors within the pixel are NMOS.

The CID pixel itself is all N-channel. Although radiation tolerance is lost, this was done in order to be able to fabricate the 32x32 Mosis array using a standard CMOS P-well 0.35 $\mu$ m process. As details for this particular array are the addition of a transfer gate and the lack of on-chip output amplifier. The pixel preamplifier has enough current capability to drive the output bus at a pixel rate up to a frequency of 1 MHz. Electrical simulation performed shows an increased dynamic range and better linearity by not using an additional on-chip amplifier.

In both architectures, transistor T2 (*row select*) can be placed either between the *row select* bus and T3 or between the *pixel out* bus and transistor T3. The first version (used in the 32x32 Mosis and 388x16 Orbit arrays) offers better overall noise performance for the array by having transistor T2 out of the noise equivalent readout chain.

### **2.2.2. The architecture of 388x16 Orbit imager**

Due to the fact that most of the results presented here are based on measurements performed on this imager, a particular emphasis will be placed on describing it. This chip was designed around the idea of a slow-read very low noise device.

Based on knowledge from previous designs, fixed pattern noise was expected to be a serious problem; therefore one major contributor (the preamplifier current source placed at the end of the column) was eliminated. In this case there is only one off-chip current source implemented as a bipolar transistor current mirror. The value of the current supplied by this is adjustable between 5 $\mu$ A and 100 $\mu$ A.

An important remark, the 388x16 Orbit imager is a typical all-PMOS fast vertical. This means Figure 2.5 appropriately describes the architecture of this array, except the current sources at the end of each column are replaced by a single off-chip current source and the pixel is a three electrode structure, the transfer gate is common for all the pixels and it runs vertically along the column.

There are a total of 16x388 pixels in the array, eight different pixel architectures grouped as eight 2x388-size subarrays. Different pixel configurations are described in section 2.3.1. The horizontal scanner is random access and the vertical one is of serial type.

Random Access Vertical Scanner (Horizontal)								Buffers/ Interface Electronics
Serial Scanner (Vertical)								
								Pixel#1 (388x2)
								Pixel#2 (388x2)
								Pixel#3 (388x2)
								Pixel#4 (388x2)
								Pixel#5 (388x2)
								Pixel#6 (388x2)
								Pixel#7 (388x2)
								Pixel#8 (388x2)

Figure 2.7 Layout sketch of the 388x16 Orbit AP-CID chip

## 2.3. Pixel architectures

Figure 2.8 shows the pixel layout for three of the arrays. For the first two arrays most of the photosensitive area is covered with thin gate oxide. In order to increase the blue response, the polysilicon electrodes cover just a fraction of the photosite. There are four vertical and two horizontal buses crossing each pixel. The photosite is considered the area covered with (thin) gate oxide, other than transistor area, where photon detection via the photoelectric effect occurs. The minority carriers generated in this region will wander around, partly being captured in the potential wells under the gates and partly being swept to the substrate by the built-in electric field of the epi-substrate PN junction.

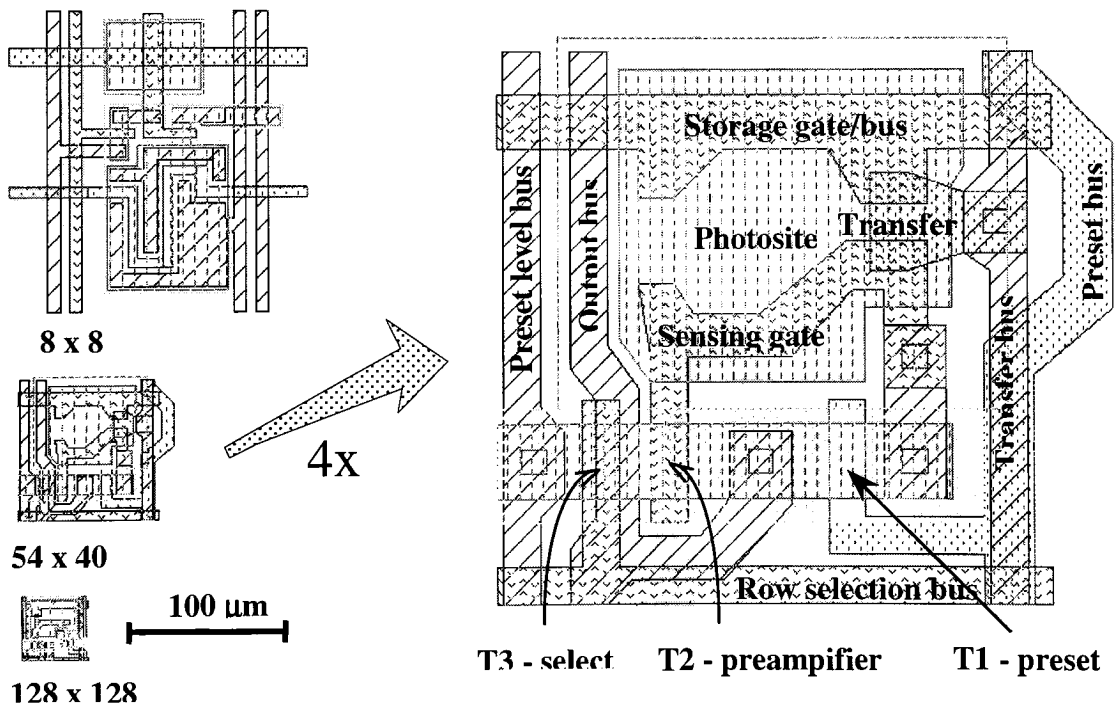


Figure 2.8 Pixel layouts for three of the AP-CID imagers

Depending on the pixel architecture, fraction of the minority carriers photo-generated in other regions of the pixel, other than the photosite, will also be collected in the potential wells.

The *design fill-factor* represents the percentage of the pixel area covered by the photosite. The photosite in case of a photodiode array represents the area of the photodiode implant. In case when the photosensitive devices are photogates (including CID's), the meaning of the photosite was extended to the area covered by thin gate oxide over which the photogates are placed.

The silicon surface under the thin gate oxide is very sensitive to radiation due to the pre-induced damage during the gate patterning by the plasma etch operation. As a consequence, while operated in harsh radiation environment, the photo-generated minority carriers will tend to be trapped at the silicon-oxide interface where most of the radiation-induced defects are located. This damage occurs to a much smaller extent in the regions covered by the gate. For optimum radiation hardness, some CID devices have to have all the gate oxide covered by the gate. As a consequence the blue/UV response for these arrays will somehow decrease since the light has to travel through a thicker layer of silicon oxide (the field oxide) in order to reach the silicon surface.

Two of the arrays (128x128 and 388x16) have thick field oxide over the photosite except under the gates. If the classical definition were to be applied, these devices would have a very low design fill factor (2-3 %). This is a misleading number since it was noticed that these devices have similar quantum efficiency with the CID devices with large gate oxide covered areas. This is due to several factors:

- the thick (1  $\mu\text{m}$ ) field oxide has a good transparency even in blue region (more than 80%)
- the minority carrier mobility in the bulk silicon material is as good under the gate as under the field oxide

The fraction of the minority carrier number which reach the potential well associated with the photo-gates is strongly dependent of other factors such as pixel size, layout, thickness

and bias voltage of the epitaxial layer on which the CID structure is built (Figure 1.7). A brief summary of the characteristics of these arrays is given in Table 2.1. Scaled pixel photographs for the same arrays are shown in Figure 2.3 (bottom).

### 2.3.1. Pixel configurations for the 388x16 Orbit imager

There are eight different pixel configurations used in this device. All pixels have a very similar structure as the 54x40 RIT pixel shown in Figure 2.8. The main difference would be that there is no gate oxide area uncovered by polysilicon gate. Even though the size of the three transistors used in each of these pixels is the same for all the pixels, the size and shape of the storage and sensing gates differ.

	Pixel#1	Pixel#2	Pixel#3	Pixel#4	Pixel#5	Pixel#6	Pixel#7	Pixel#8
Pixel size [ $\mu\text{m} \times \mu\text{m}$ ]	27 x 27	27 x 27	27 x 27	27 x 27	27 x 27	27 x 27	27 x 27	27 x 27
Pixel area [ $\mu\text{m}^2$ ]	729	729	729	729	729	729	729	729
Sense gate area [ $\mu\text{m}^2$ ]	7.2	14.4	29	52	7.2	7.2	14.4	14.4
Storage gate area [ $\mu\text{m}^2$ ]	7.2	14.4	29	52	29	55	93	95
Transfer gate area [ $\mu\text{m}^2$ ]	6.7	6.7	6.7	6.7	6.7	6.7	6.7	6.7
Preamplifier Size [W/L]	3.6/1.6	3.6/1.6	3.6/1.6	3.6/1.6	3.6/1.6	3.6/1.6	3.6/1.6	3.6/1.6
Sense/store gate material	Poly_2	Poly_2	Poly_2	Poly_2	Poly_2	Poly_2	Poly_2	Poly_2
Transfer gate material	Poly_1	Poly_1	Poly_1	Poly_1	Poly_1	Poly_1	Poly_1	Poly_1
Sense gate cap. [fF]	4.5	9	18	32	4.5	4.5	9	9
Storage gate cap. [fF]	4.5	9	18	32	18	34	58	59
Transfer gate cap. [fF]	11	11	11	11	11	11	11	11
Sense well capacity [e/V]	45,000	90,000	180,000	325,000	45,000	45,000	90,000	90,000
Measured full well cap.[e]	35,000	91,000	176,000	252,000	52,000	47,000	72,000	92,000

Table 2.2 Parameters of eight different types of pixels used in 388x16 Orbit AP-CID

The different gate geometries/shapes were chosen in order to investigate the effect of pixel parameters on characteristics such as *readout noise*, *gain*, *linearity*, *fixed pattern noise*, *shading*, *dark current*. The following two figures shows the layout of various pixels used in the array and Table 2.1 summarizes some of the characteristics of these pixels.

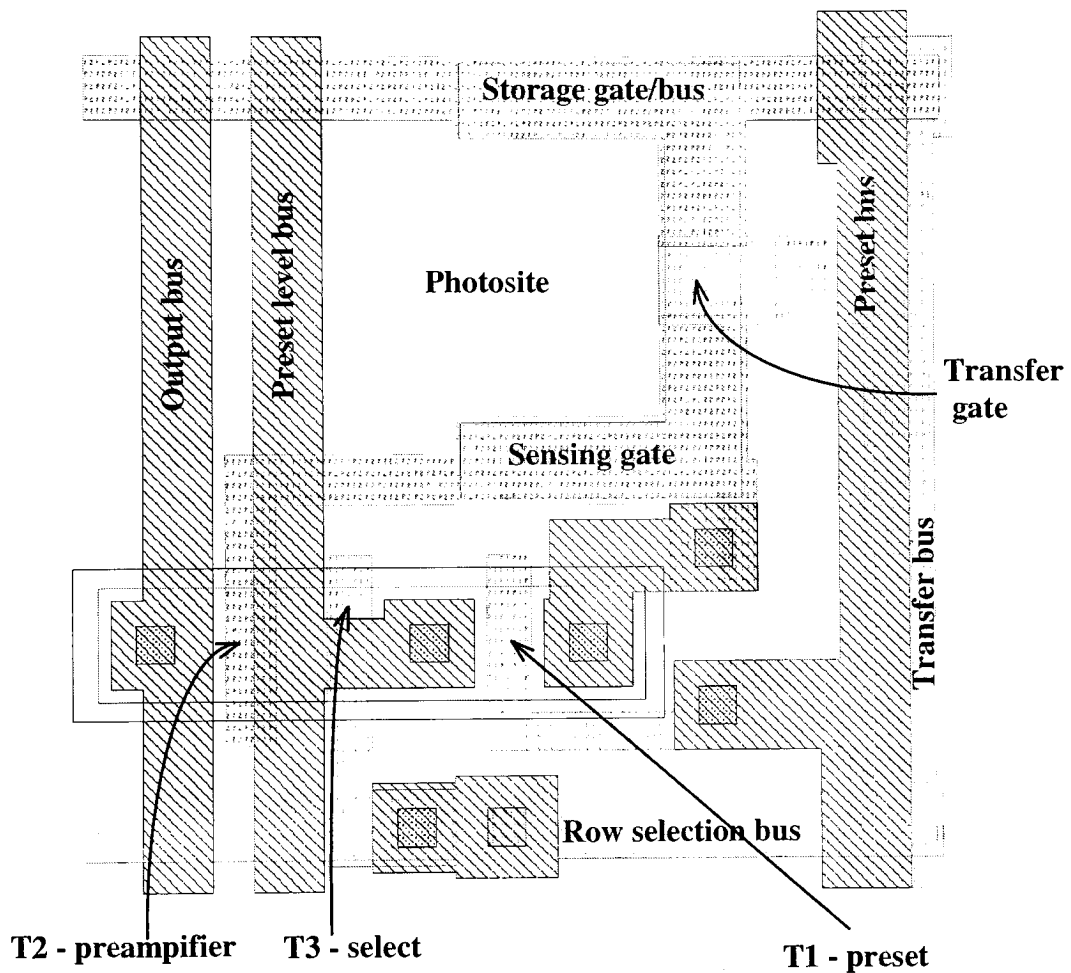


Figure 2.9 Layout of pixel#3 of 388x16 Orbit AP-CID array

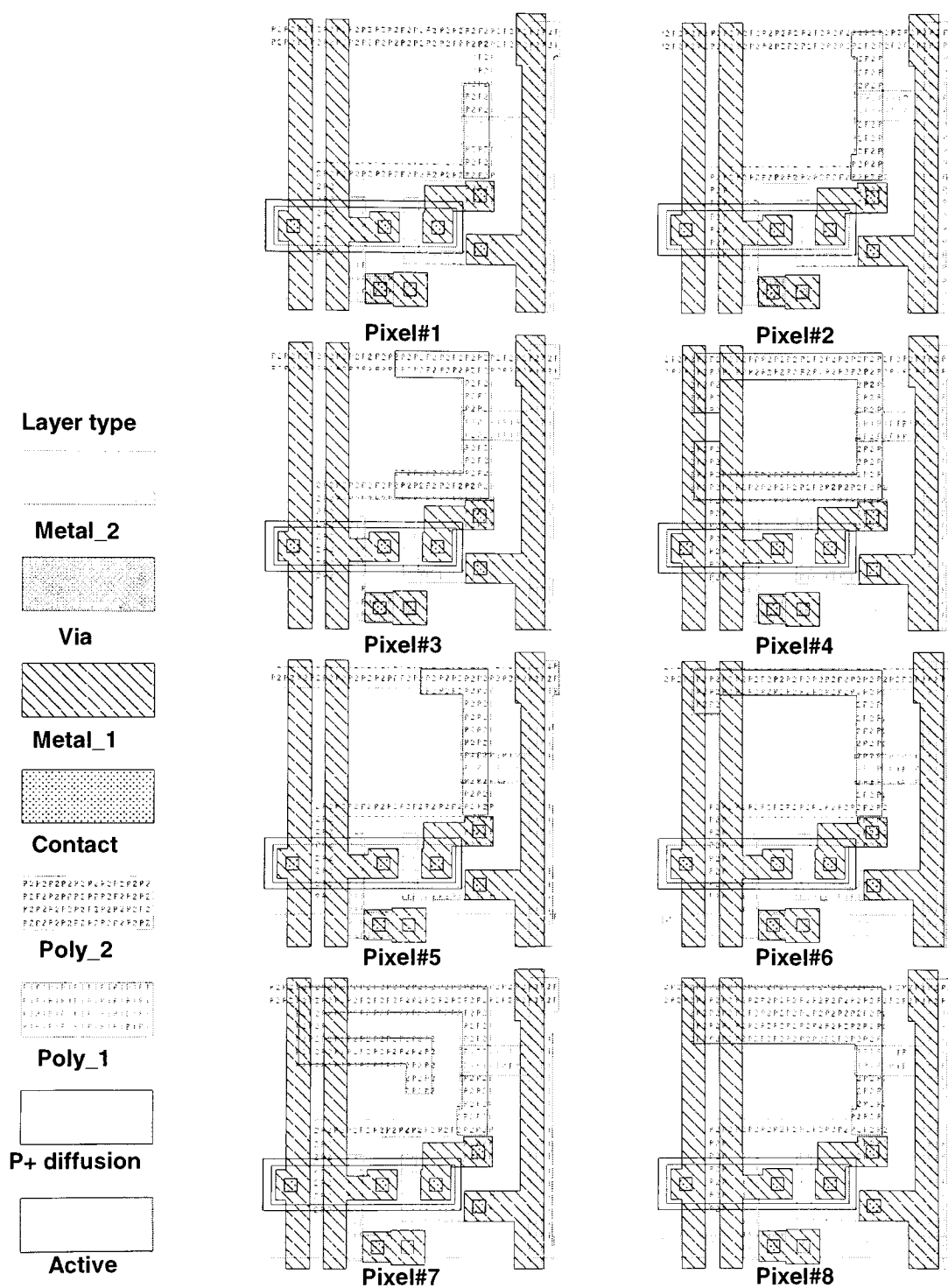


Figure 2.10 Eight different pixel configurations used in the 388x16 Orbit AP-CID

## 2.4. Full-frame array operation

The CID imager is well known for flexibility in operation<sup>21</sup>. Special readout modes can be employed such as: readout of random region of interest as well as the injection of random regions of interest, skimming (partially injecting certain pixels), or random pixel binning (reading out the average signal from a group of pixels). A good understanding of the basic full-frame operation/readout algorithm would allow one to derive more sophisticated ways of extracting image information from an AP-CID.

### 2.4.1. Modes of operation

In order to avoid redundancy, several aspects are important to mention about the array operation as described here.

- *Column readout is assumed.* If an arbitrary array has row readout just by rotating it by 90 degrees, the operation of the array can be appropriately described by one of the modes described here.
- *Rows run horizontally and columns vertically.*
- *Vertical scanner is synonymous to row scanner, horizontal scanner is synonymous to column scanner.*
- *There are possible two readout modes: fast vertical and fast horizontal.*
- *There are possible two injection modes: frame inject and row inject.*
- *Both two-electrode and three-electrode pixel architectures can be employed in either mode of readout or either mode of injection.*

The logic diagram describing a P-channel fast-vertical AP-CID architecture is presented in Figure 2.11. A three-electrode pixel structure is assumed. As a reference, the phases of operations for this structure are shown in Figure 1.9.



Operation step	Storage gate	Transfer gate	Sensing gate	T1	T3	T5	Preset level	Operation level
Light integration	0V	4.5V	0V	On	*	*	0V	Frame
Back transfer	0V	4.5V	5V	On	*	*	5V	Column
Preset	0V	4.5V	0V	On	*	*	0V	Column
Readout_1	0V	4.5V	Float.	Off	On	On	0V	Pixel
Forward transfer	5V	4.5V	Float.	Off	*	*	0V	Row
Readout_2	5V	4.5V	Float.	Off	On	On	0V	Pixel
Clear/Inject	5V	5V	5V	On	*	*	5V	Frame

Table 2.3 Voltage diagram representing the operation of a P-channel three-electrode per pixel fast-vertical readout architecture AP-CID. (\*State irrelevant)

The cycle starts with the charge injection in all the pixels, followed by light integration. Then, the first column of the array is selected and the charge from the storage electrode is transferred to the sensing electrode (*back transfer*) all along the selected column. At this point, there is no electric charge left in the potential wells corresponding to the sensing gates and the gates are set in charge collection mode or preset mode (typically a potential of 0V is applied on all the sensing gates for a P-channel device).

After this, the first row is selected, and the sensing gates on this row are left floating. Readout is done. The charge is then transferred from the storage to the sensing well all along the selected column. A second readout is done. The voltage difference between the two readouts is proportional to the photo-generated charge from the first pixel of the first column. The second row will follow the same readout sequence. This way, all the pixels of the first column are readout.

After each column is read, there is a new back transfer of electric charge from the sensing wells to the storage wells followed by the readout of each pixel in the following column. Finishing the last column, the cycle repeats itself starting with the charge clear operation and light integration. It should be mentioned that a two-electrode pixel structure could be operated with almost the same sequence.

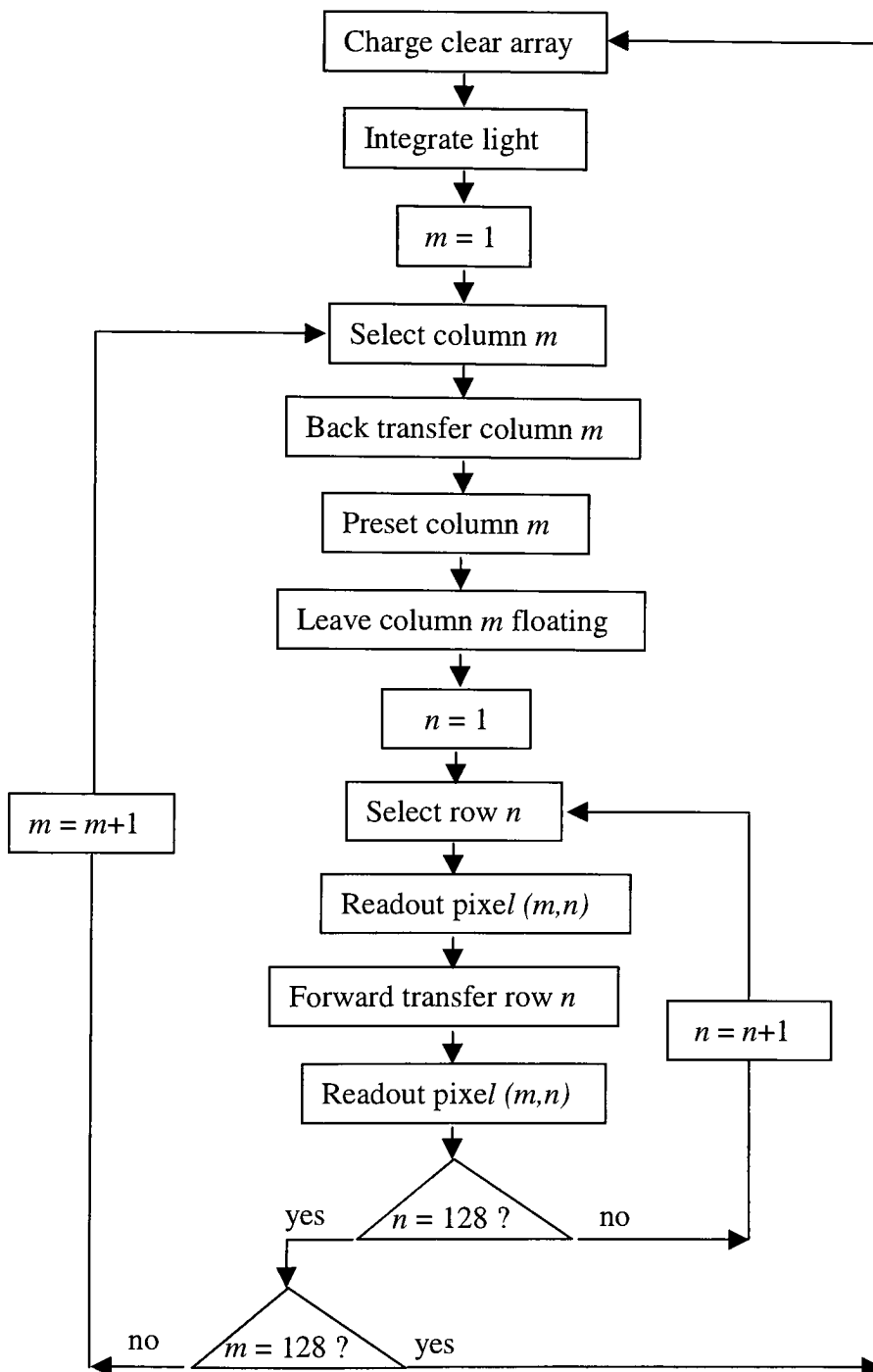


Figure 2.11 The logic diagram for operation of a fast-vertical scanning 128x128 AP-CID architecture having three electrodes per pixel

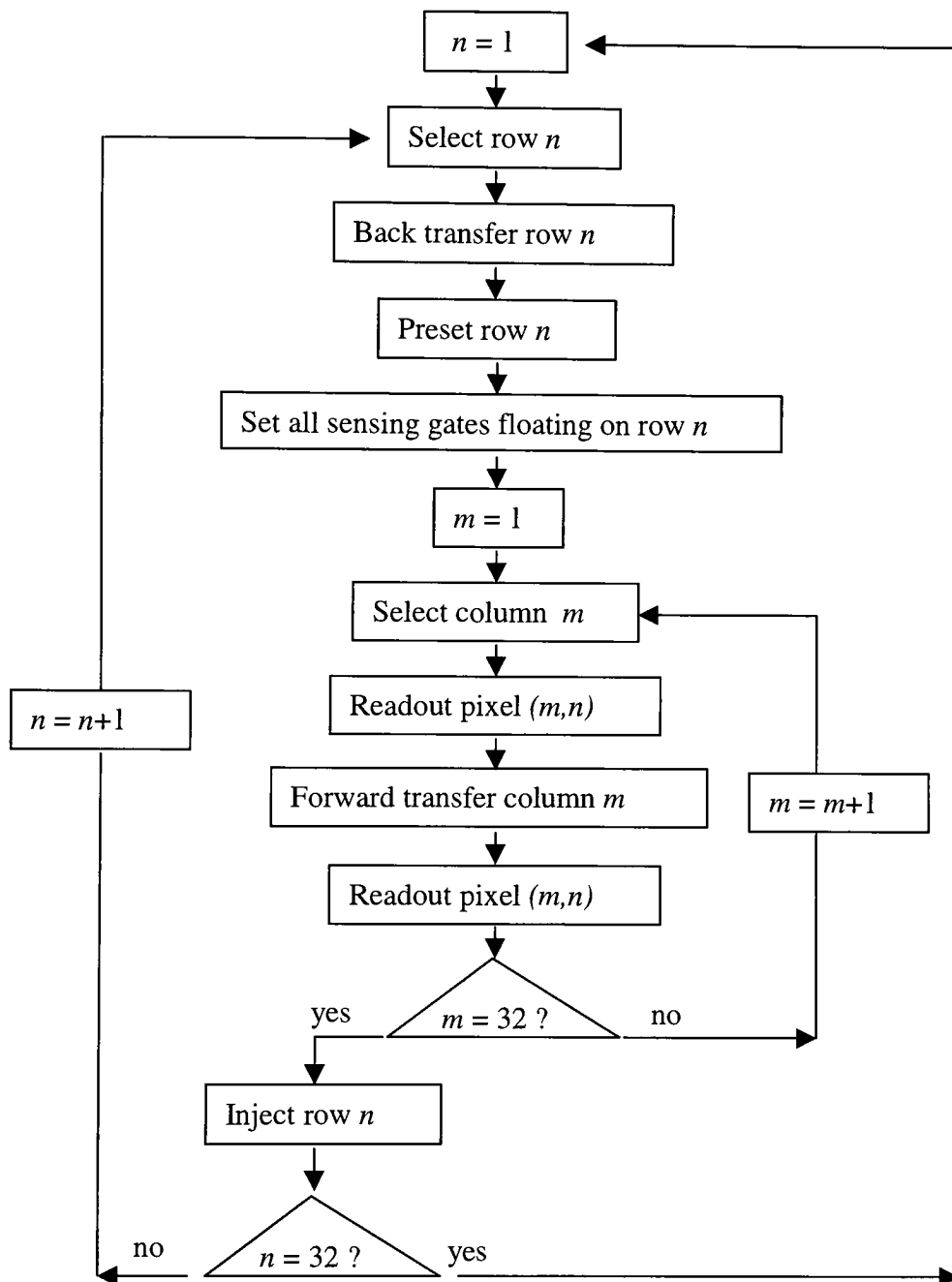


Figure 2.12 The logic diagram for the operation of a fast-horizontal scanning 32x32 AP-CID architecture having three electrode per pixel

The only difference is that (see Figure 1.8) there is no need for the back transfer phase (due to the well depth difference, the charge automatically “flows” from the sensing well to the storage well during the phase of light integration).

Another important observation is that the fast-vertical architecture can be operated in a column-injection mode. This mode of operation is typically employed while the AP-CID camera is operated in a video mode without a shutter.

Table 2.3 contains the voltages on the gates and the state of the transistor switches for a three-electrode P-channel AP-CID in various phases of operation, and it should be referenced with Figure 2.5.

The logic diagram describing the operation of an N-channel fast-horizontal scanning AP-CID architecture is presented in

Figure 2.12. A three-electrode pixel structure is assumed. A row injection mode of operation (unshuttered exposure) is presented here, although the same architecture can be operated in a frame injection mode.

Figure 2.6 is to be referenced with this mode of operation for this architecture.

The cycle starts with the selection of the first row. The charge from all the sensing potential wells (connected together by a row bus) is transferred under the storage potential wells (*back transfer*) in all the pixels along the selected row. The row is then preset. This way a potential well is formed corresponding to the sensing gate which is now empty. The sensing electrodes are left floating along the whole row and the first column is selected. A first readout is done. Then the electric charge along this first column is transferred from the storage potential well to the sensing potential well followed by another readout. The difference between the two output readout voltages is proportional to the electric charge stored in the first pixel of the array. The second column will follow the same readout sequence. This way, all the pixels along the first row are readout in a serial fashion. At this point the whole row will be injected (charge cleared).

Then the second row is being selected. A back transfer is done followed by a serial readout of all the pixels along this row. Finishing the last row, the cycle repeats itself.

It is important to observe the lack of a dedicated light integration period. Actually the light integration time for this particular sequence is equal to the frame readout time (the time between consecutive injections for any given pixel). Such a step could be added if there is the need to expose the array longer than the readout time (such as using the array in astronomy at very low light levels and long exposure times).

By using a shutter, the array could be operated in a frame injection mode. Two steps have to be added to the sequence: the exposure period and the frame injection period. Obviously the row injection stage can in this case be missing.

An important remark here is that the maximum pixel readout frequency for both architectures is around 50 to 100 kHz. In this case few tens of microseconds are needed to drive the output capacitance node to the proper potential while a new row is selected. For the fast horizontal architecture this speed could be two-three orders of magnitude higher if the storage bus is made vertical. In our case this is not the case. Both architectures can be made that fast by adding an analog processing block at the end of the column or row respectively (for the vertical or horizontal architecture respectively). This topic is however beyond the scope of this thesis.

It should be mentioned that a two-electrode pixel structure could be operated with almost the same sequence. The only difference in terms of operation sequence is that (see Figure 1.8) there is no need for the back-transfer phase.

## **Chapter 3. Experimental**

### **3.1. Imaging hardware**

In order to perform valid measurements with the above mentioned device ancillary electronics was built. All the electronics used to drive the imager and to condition and amplify the output signal coming from the imager is generically called “the camera” in the industrial imaging community. This includes power supplies, amplifiers, logic circuits, A/D converter, level translators, buffers, CDS circuit etc.

#### **3.1.1. The camera**

Three versions of the camera were built since April 2002. The last version (used to obtain most of the results) will be presented here. A block diagram and a photograph of this camera are presented in Figure 3.1.

On the right side of the block diagram there is the power module. There are nine different stabilized and adjustable power supplies. A rotary switch (black) makes it easy to measure any of the voltages with a four-digit display meter. The power module also contains a clock generator. Another rotary switch (red) can select various frequencies supplied by a frequency divider.

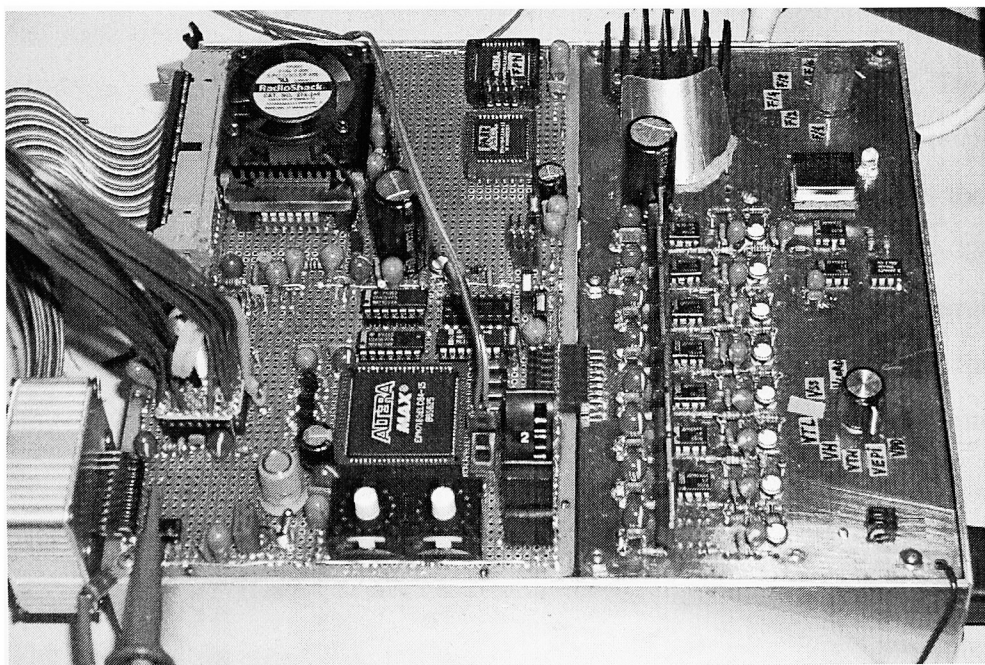
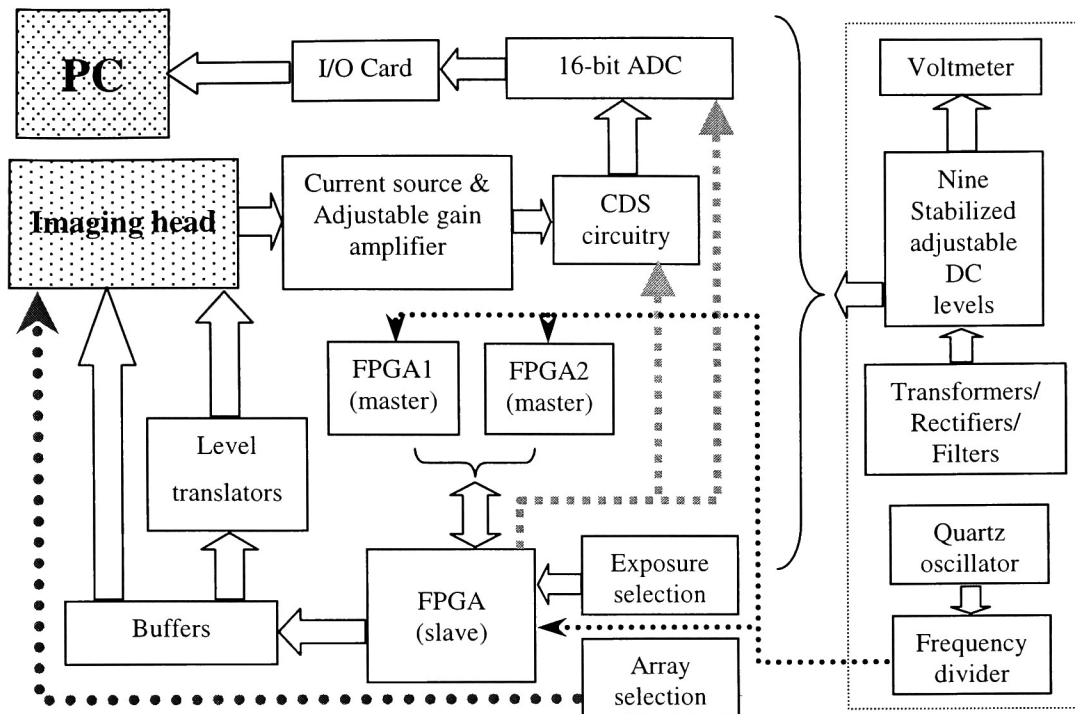


Figure 3.1 Block diagram and photograph of the camera for 388x16 Orbit imager

The slave FPGA (field programmable gate array) is the imager driver. This circuit contains all the information the imager needs to run in any mode of operation.

There are three main “slave” modes of operations: integrate, inject and readout. The readout has included in it the “back transfer” phase. Though the slave FPGA could run alone, another “master” FPGA is used to control it. The reason for doing this is flexibility. The slaves are small FPGA circuits dedicated for each type of experiment (normal continuous operation, dark current measurement, quantum efficiency measurement, mean variance measurement, linearity measurement, FPN measurement, etc). They are placed in sockets and are easy to swap while switching from one type of measurement to another. There are two slave FPGA’s on the board but there is a switch selecting only one at a time. A handshaking procedure allows communication between the master and the slave.

The master gives a “request” code, which tells the slave which kind of operation to perform. When finished the slave sends back an “acknowledge” signal so that the master can issue a next “request” code.

Complex measurement algorithms have been implemented this way. To avoid transitory effects the imager is continuously clocked at power-up. However there are two switches on the board (one for each “master” FPGA), which synchronize the data acquisition operation.

The slave FPGA is connected to a binary thumb switch, which controls the exposure time. Another thumb switch connected directly to the imager controls the type of pixel used in a certain experiment. Both these switches offer flexibility in measurement but can be, at times, overridden by either of the master FPGA.

The slave FPGA is interfaced with the imager through a series of buffers and level translators.

The output of the imager is sent to a current source and then to an amplifier. The amplifier is of the noninverting type and has three settings for the gain: 9.27, 13.12 and 28.42. The lowest gain is used in most of the experiments. The middle gain was used in



quantum efficiency measurements and the highest gain was used in mean-variance (gain and noise) measurements.

After the gain stage the signal can be displayed on an oscilloscope and it's also sent to a correlated double sampling (CDS) circuit (the small aluminum box on the lower right corner of the picture). Between the amplifier and the CDS circuit a low pass filter is inserted. This is a simple RC filter having one single pole situated close to pixel frequency.

The CDS circuit clamps to ground the first sample of any pixel (before transfer value) and holds the second sample (after transfer value).

After that, the correlated double sampled signal is transferred to a 16-bit *Analogic ADC4325* analog to digital converter (ADC). The output of this converter is connected to a *National Instruments AT-DIO-32F* I/O card inserted in a PC. The slave FPGA clocks the CDS circuit, ADC and the I/O card.

The setup together with the imager was proven to run at almost 100 kilopixel/second. However the I/O card started to malfunction beyond 18 kilosamples/second. During all the experiments the setup was run at 16.7 kilopixel/second.

### **3.1.2. The imaging head**

The imager was mounted in an anodized aluminum case provided with a quartz optical window. Inside the case there is a 3-stage “*Melcor*” thermoelectric cooler (model 3CP-085-065-127-71-31 – 8.4A/15.4V/89°C). Due to the fact that the TE cooler dissipates more than 120W of power when operated at maximum capacity, the head was water-cooled using a fish-tank centrifugal pump.

Temperatures lower than  $-50^{\circ}\text{C}$  at the imager level are possible to attain with this setup. Lower temperatures are possible by adding ice cubes to the cooling water. The only

problem at low case temperatures would be the formation of dew on the case, connectors and optical window.

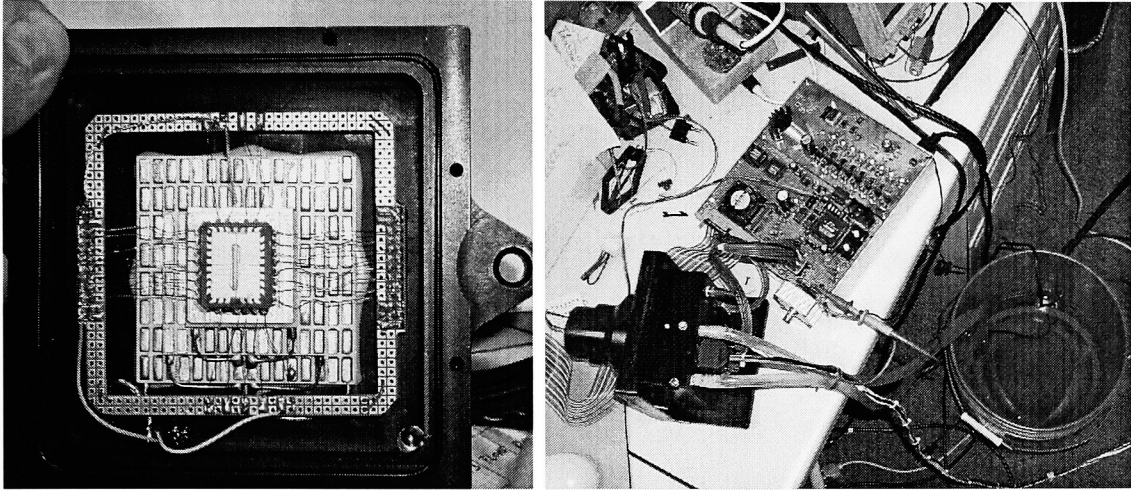


Figure 3.2 Open imaging head case with 3-stage TE cooler (a), water cooling setup for 388x16 AP-CID imaging head (b)

Figure 3.2 (a) shows the imaging head before being vacuumed. The 3-stage TE cooler can be seen behind the imager. Figure 3.2 (b) shows the whole system together with the cooling tubes and the water container.

The chip is bonded on the same carrier with a “*Fenwal*” thermistor for temperature monitoring. A look-up table allows temperature calculations by knowing the resistance of the thermistor.

## **3.2. Transfer characteristic (TC) curve measurements**

### **3.2.1. Background**

The fundamental process that occurs in electronic imaging is the conversion of the photonic input to electronic output. Photons incident on the active area of the device (pixels) will be converted to electron/hole pairs and the holes will be captured under the photogates of the CID. These photo-generated charge carriers will determine a voltage change in the output of the pixel preamplifier. An analog processing chain further amplifies this signal, which is finally digitized before being transferred to a host computer for display/image processing, and/or storage.

It is very important to know the relationship between the output level of the device (in this case the output of the analog to digital converter) and the amount of exposure. Ideally this relationship is linear, the more exposure the array is subjected to, the larger the output signal. In any real case there are deviations from this rule. An important aspect to mention is that the range of the output signal is limited therefore there is a maximum exposure level beyond which the output level of any camera will saturate. In typical CCD cameras the TC curve is very linear for small signals and nonlinear around the saturation. Nonlinearity in the APCID array will be analyzed in section 3.5.

A particular aspect, characteristic to three-electrode CID pixels, is the fact that the TC curve doesn't remain flat after saturation but starts falling off after a certain exposure interval from the saturation point depending on the pixel architecture and the electrode bias voltage. The camera starts exhibiting a negative gain after saturation by which very bright pixels can appear darker than dimmer ones. It is a parasitic effect and means of controlling it will be analyzed.

### 3.2.2. Experiment

The measurement requires that the imager be successively run with increasing levels of exposure. Between the zero-exposure point (dark) and the maximum-exposure point (full well capacity), a series of image frames (in this case 40) are captured. The imager is illuminated with a stabilized and diffuse light source (LED), far enough from the device so that the exposure is uniform within the array plane. The exposure level is controlled by time modulation. Thermoelectric cooling (around  $-20^{\circ}\text{C}$ ) of the array is employed.

Data is taken from twelve consecutive series of exposures. Because each array has 400 pixels there will be available 4800 digitized output values for each of the 40 exposure points. The last 12 data output points are discarded from the computation in each frame. They have a very low digital count (no image information). This “data blanking” technique is used in order to easily identify the end of each frame while saved in text format. The pixel rate is 16.7KHz.

A row average (388 pixels) is calculated for each exposure level, by using an Excel spreadsheet, then plotted versus a relative exposure time.

### 3.2.3. Results and discussion

Overlaid transfer characteristic curves for the eight different arrays are presented in Figure 3.3. Individual plots for each pixel are available in Figure 3.17. A TCC for a typical solid state sensor has two different regions. The first part is called *the linear region*. It starts at the origin, is fairly linear and has a positive slope. It is where the usable imaging process occurs. The slope of this region is proportional to the gain of the imager

and the quantum efficiency (section 4.1.1). The second part is called saturation and the curve reaches its maximum within this section.

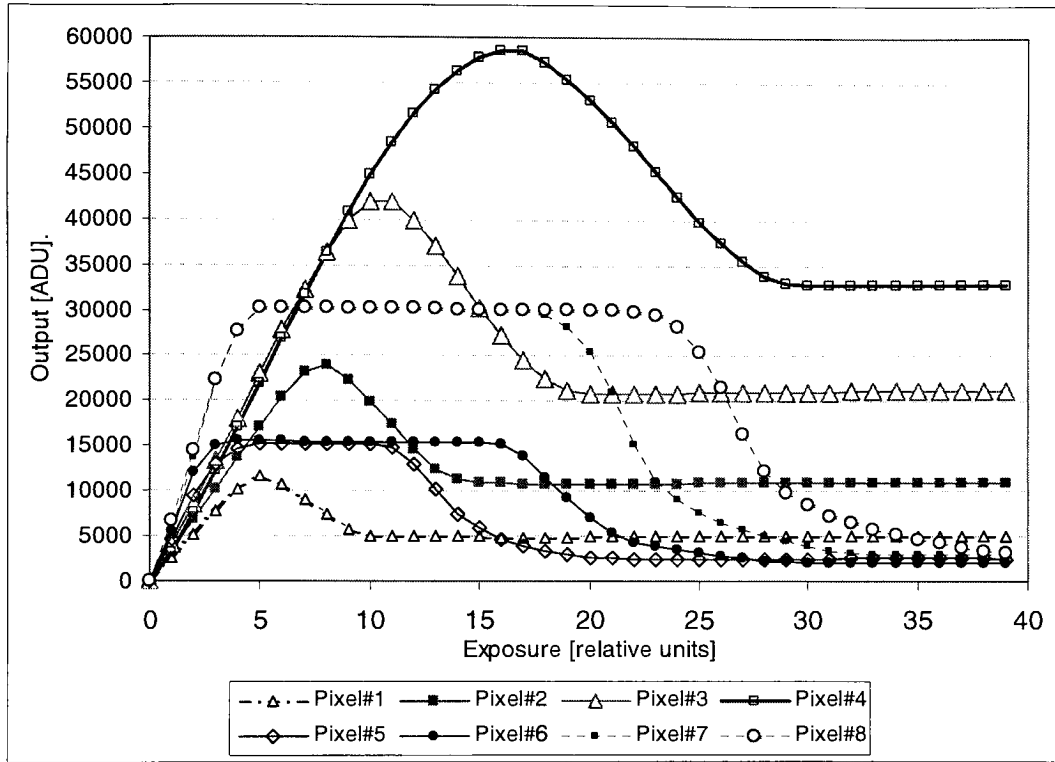


Figure 3.3 Transfer characteristic curves for different pixel architectures

Two-electrode CID pixels have a flat output at saturation but as we can see in this present experiment the three-electrode pixel structure behaves differently.

The saturation region has three parts: a flat maximum region, a second region with negative derivative followed by a constant minimum. It seems that the constant maximum region is very short for pixels with equal area sensing and storage gates, increasing with the area of the storage gate. Another important observation is that the ratio of the saturation maximum and the saturation minimum is roughly equal to the ratio between the area of the storage gate and the area of the sensing gate.

Finally it is important to notice that the output swing varies with the area of the sensing gate. Both these phenomena will be analyzed in section 4.1 of this thesis.

### 3.3. Gain and noise measurements

#### 3.3.1. Method

In order to determine the readout noise and the gain of the imagers, the photon transfer method as described by Janesik is employed<sup>33</sup>. The output variance of the signal  $V(S)$  (in analog-to-digital units (ADU) squared) after digitization, is related to the signal level  $S$  (in ADU), the r.m.s. noise floor  $N_r^2$  (in electrons) and the gain  $g$  (digital counts/electron) by the following formula:

$$V(S) = g^2 N_r^2 + gS \quad (3.1)$$

The variance plotted versus the signal level is called the *photon transfer curve* or *mean-variance curve*.

#### 3.3.2. Experiment

Using flat field images taken at various exposure settings, values for the average signal level  $S$  and signal variance  $V(S)$  can be computed.

The measurement is done while the imaging chip thermoelectrically cooled at  $-30^\circ\text{C}$  and it is being illuminated with a stabilized LED. A series of 10 image frames (388 image pixels + 12 blanking pixels) are taken, each at increasing exposure levels. The

procedure is repeated 16 times. For each pixel configuration at any exposure level, the variance (over 16 values) in the output signal is calculated. An average of the pixel variance across the whole frame is computed for each exposure level. That represents  $V(S)$ . An average for all the pixels is also calculated for each exposure level, and this represents  $S$ . The photon transfer curve  $V(S)$  is then plotted.

A least square fit can be applied to the above data and the slope of this curve gives the gain  $g$ . Knowing the gain, the noise floor (readout noise) can be calculated using the standard deviation at zero signal (dark readout) and dividing by the gain.

### 3.3.3. Results and discussion

A mean-variance plot for pixel#1 is presented in Figure 3.4. A full set of mean-variance plots for all the pixel configurations is found in Figure 3.18.

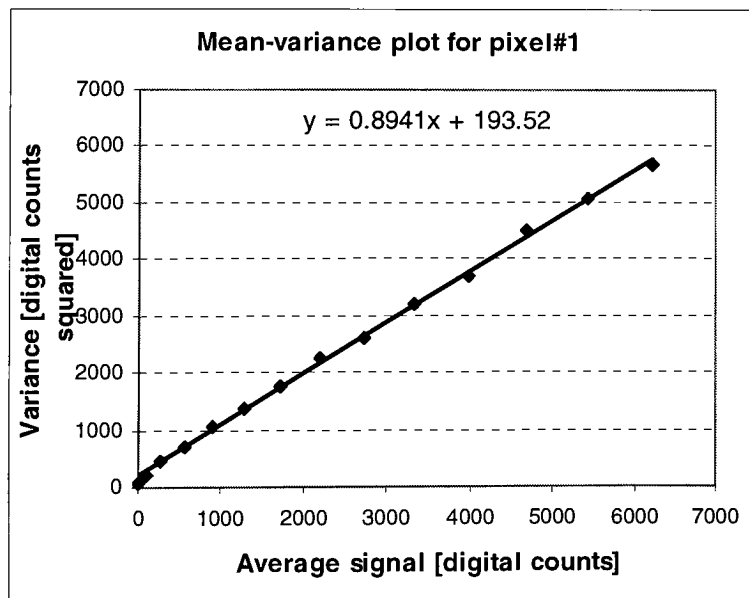


Figure 3.4 A mean-variance plot for pixel#1

Due to the nonlinearity of the device, the inject noise (section 1.6.5), and the fact that the readout noise in complete darkness is so small, the intercept of the linear fit curve will not be equal to the variance corresponding to the dark frame. The variance of the dark frame will represent the preamplifier readout noise and the intercept will represent the injection noise. For this reason the variance of the dark frame will be used to calculate the readout noise.

### 3.4. Full well capacity and dynamic range calculation

The full well capacity represents the maximum number of minority carriers that can be stored under the sensing gate (at saturation). It can be calculated by dividing the maximum output signal range by the gain.

$$FullWellCapacity = \frac{OutputSignalRange}{Gain} \quad (3.2)$$

It is important to regard the previous definition with caution since it is defined for a perfectly linear imager. For real imagers, the full well capacity calculated with this formula will be smaller than the actual one.

The dynamic range is calculated as the ratio of the full well capacity and the readout noise level. This parameter can be regarded as the maximum number of gray levels discernable in an image obtained using the camera under test.

$$DynamicRange = \frac{OutputSignalRange}{ReadoutNoise} \quad (3.3)$$

A summary of the results is listed in the table below.



	Full well capacity	Dynamic Range	Dynamic Range [dB]
Pixel#1	35,040	4,972	74
Pixel#2	90,844	9,944	80
Pixel#3	175,784	17,347	85
Pixel#4	252,000	30,660	90
Pixel#5	52,748	7,665	78
Pixel#6	46,720	6,541	76
Pixel#7	72,425	13,140	82
Pixel#8	92,909	13,140	82
Average	102,309	12,926	82

Table 3.1 Outline of the gain and readout noise measurement results

## 3.5. Linearity

### 3.5.1. Method

The average digitized output from a solid state imager should vary linearly with the amount of light incident on the device. Hence non-linearity is a measure of the deviation from the following relationship:

$$Digital\_Signal = A \times Exposure + B \quad (3.4)$$

where A and B are constants.

High performance CCD imagers have good linearity, exhibiting less than a few tenths of a percent non-linearity over five orders of magnitude of dynamic range. Commercial CCD's and APS devices often behave worse (typically few percent non-linearity). For quantitative imaging, linearity is a very important requirement enabling image operations such as arithmetic ratios, shading and fixed pattern noise correction, flat fielding and linear transforms.

There are various methods for measuring or reporting linearity. One of them is to plot the mean signal value versus the exposure time over a part of the dynamic range that can be considered the most linear (typically somewhere between 0% and 90% of dynamic range). A linear least square regression is fit to the data.

The maximum error in the signal (the maximum distance between any one experimental point and the linear fit curve added to the maximum negative distance between any experimental point and the linear fit) is the linearity and it is expressed in percentage of the maximum signal.

The following two formulas express the nonlinearity/linearity:

$$Nonlinearity = \left( \frac{MaximumDeviation}{MaximumSignal} \right) \cdot 100 \quad (3.5)$$

$$Linearity = 100 - Nonlinearity \quad (3.6)$$

### 3.5.2. Least square regression

Suppose we have  $n$  pairs of points  $(x_i, y_i)$  plotted on a chart. If a straight line could be found to connect the points exactly we would call this a perfect fit. In most of real imaging situations the points are not aligned therefore, such a line doesn't exist. A “least square” approximation can be used to find the equation of this line as follows.

If the equation of the line is:

$$y = ax + b \quad (3.7)$$

the squared fitting error will be :

$$\Sigma^2(a, b) = \sum_{i=0}^{n-1} (y_i - ax_i - b)^2 \quad (3.8)$$

In order to find the slope and the intercept of the linear fit the partial derivatives of this error function with respect to “ $a$ ” and “ $b$ ” have to be equal to zero. Therefore a system of equation is formed:

$$\begin{cases} \frac{\partial \Sigma(a, b)}{\partial a} = 0 \\ \frac{\partial \Sigma(a, b)}{\partial b} = 0 \end{cases} \quad (3.9)$$

Simple algebra leads to the result:

$$\left\{ \begin{array}{l} a = \frac{n \sum_{i=0}^{n-1} (x_i y_i) - \sum_{i=0}^{n-1} x_i \sum_{i=0}^{n-1} y_i}{n \sum_{i=0}^{n-1} x_i^2 - (\sum_{i=0}^{n-1} x_i)^2} \\ b = \frac{\sum_{i=0}^{n-1} y_i - a (\sum_{i=0}^{n-1} x_i)^2}{n} \end{array} \right. \quad (3.10)$$

### 3.5.3. Experiment

The measurement requires that the imager be successively run with increasing levels of exposure. Between the zero-exposure point (dark) and the maximum-exposure point (full well capacity), a series of image frames (in this case 40) are captured. The procedure is repeated twelve times. The imager is illuminated with a stabilized and diffuse light source (LED), far enough from the device so that the exposure is uniform within the array plane. The exposure level is controlled by time modulation. Thermoelectric cooling (around  $-20^{\circ}\text{C}$ ) of the array is employed.

Because data is taken from twelve consecutive series of exposures and because each array has 400 pixels each of the 40 points of the linearity plot will be the average of 4800 digitized output values. The last 12 data output points are discarded from the computation in each frame. They have a very low digital count (no image information). This “data blanking” technique is used in order to easily identify the end of each frame while saved in text format. The pixel rate is 16.7KHz.

A frame average is calculated for each exposure level, by using an Excel spreadsheet, then plotted versus a relative exposure time. A linear regression is performed using the formulas in section 3.5.2.

The difference between the linear fit curve and the data points represents the fitting error and is plotted against the relative exposure. The maximum error is detected and used to calculate the nonlinearity (equation 3.5).

Several intermediate exposure ranges from zero to  $x$  (where  $x$  is smaller or equal than 90% of the signal range) are selected for which the nonlinearity is calculated. A graph of nonlinearity versus signal range is plotted for each type of pixel.

### **3.5.4. Results and discussion**

Figure 3.5 Shows the transfer characteristic of two pixels. Pixel#7 is the most nonlinear pixel of the array. There is an obvious convexity in the low light level of this curve, which gives a high nonlinearity to start with. This phenomenon is barely present for pixel#2, which has the same size and shape sensing and transfer gate. We can assume that this is a transfer efficiency issue for low light levels. This is due to the fact that the storage gate is more than six times larger in pixel#7 than in pixel#2, and the storage gate of pixel#7 is tortuous. As a matter of fact the best linearity at low light level is by pixel#1, which has small and almost square storage/transfer gates, hence the best transfer efficiency.

In the upper part of the transfer characteristic for pixel#7 there is a serious decrease in the slope of the transfer characteristic. This will be proven later (section 4.1.2.3), and it is due to charge sharing between the sensing gate and the storage gate. This change in slope of the characteristic curve is one of the reasons for increased nonlinearity at high light levels.

At high output levels there is a nonlinearity contribution from the preamplifier. This will be analyzed further but it is expected to be more of an issue for pixels with larger sensing gates. These pixels have a larger range of the output signal.

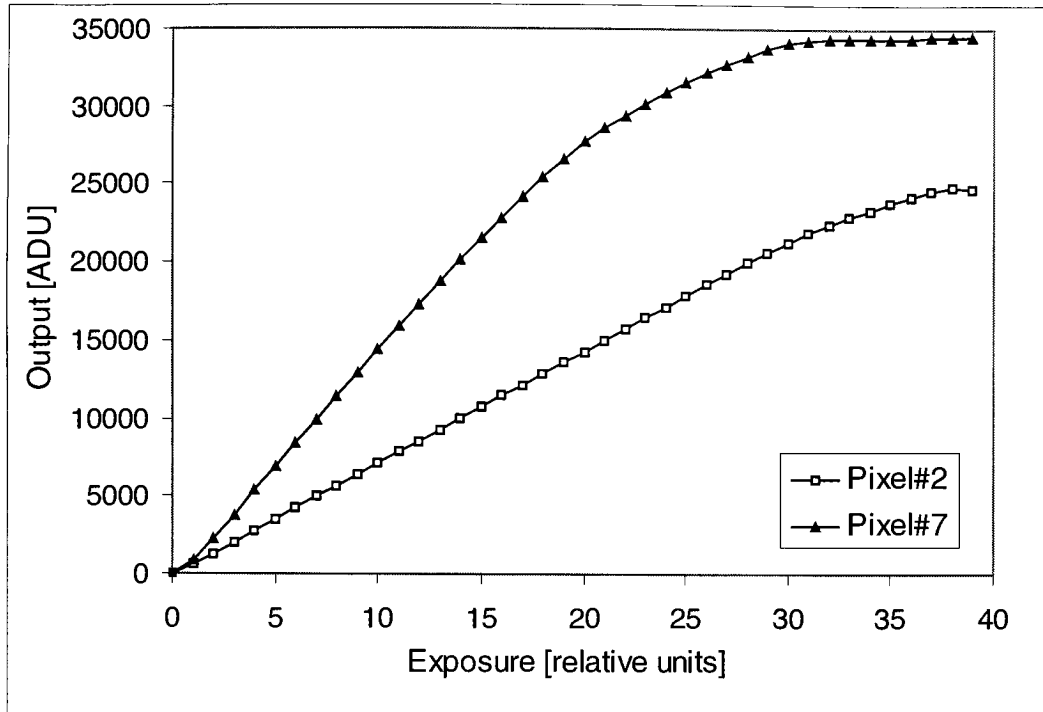


Figure 3.5 TC curves for two different pixels, pixel#1 (the most linear) and pixel#7 (one of the most nonlinear)

Figure 3.6 shows the nonlinearity of the each pixel type function of the output signal range over which this parameter is calculated. The curves show a region around 65%-80% of the total output range for which the linearity is optimum (less than 2%).

It is visible from Figure 3.6 that all the different pixels have a minimum in nonlinearity around 60 to 80% of the dynamic range. In applications, which require good linearity, the maximum signal should be specified around that region. As a conclusion, the AP-CID can be designed to have less than 1% nonlinearity over 80% of the dynamic range which is as good a number as nonlinearity of passive versions of CID devices.

At high output levels there is a nonlinearity contribution from the preamplifier. This will be analyzed further in section 4.3 but it is expected to be more of an issue for

pixels with larger sensing gates because these pixels have a larger range of the output signal.

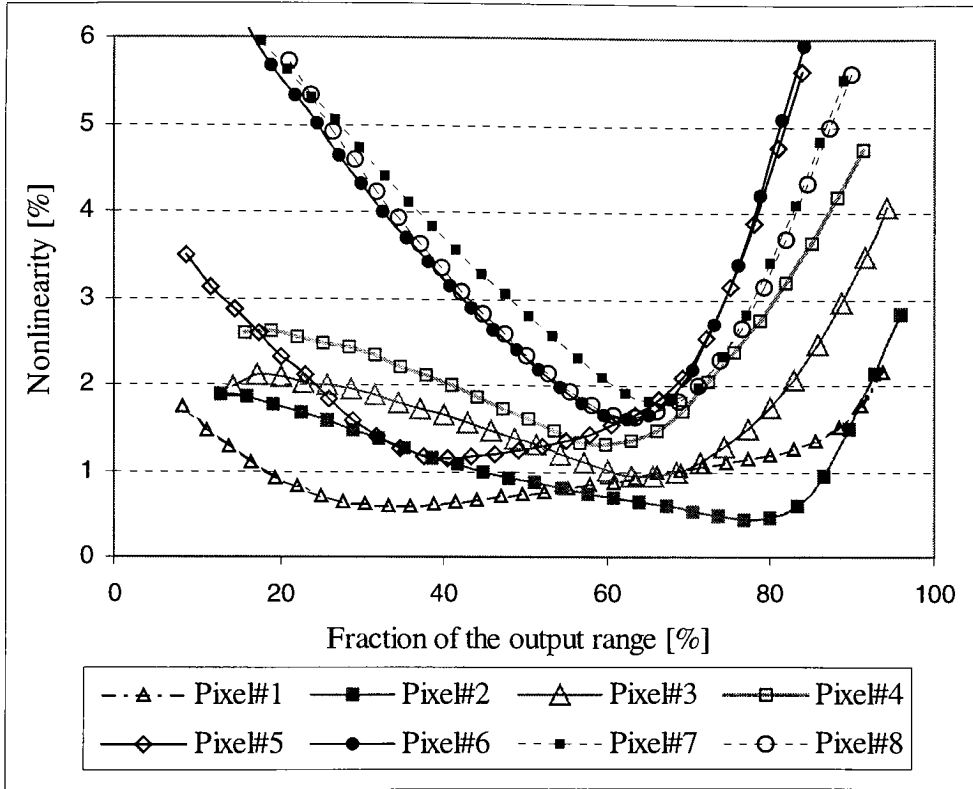


Figure 3.6 Variation of nonlinearity with the output signal range for different pixel architectures

## 3.6. Quantum efficiency

### 3.6.1. Method

Quantum efficiency  $\eta$ , is defined as the number of minority carriers collected under the photogates divided by the number of photons impinging on the device. Considering a P-channel device, the number of holes contained under the sensing gate at the readout can be written function of the gain and the signal level:

$$number\_of\_holes = g \cdot S \quad (3.11)$$

The number of photons impinging on the pixel area  $A_{pixel}$  within the integration time  $T_{int}$  while the imager is exposed to an irradiance level  $E_\lambda$  can be written as

$$number\_of\_photons = \frac{E_\lambda \cdot A_{pixel} \cdot T_{int}}{photon\_energy} \quad (3.12)$$

The energy of a photon of frequency  $\nu$  and wavelength  $\lambda$  can be written as

$$photon\_energy = h \cdot \nu = \frac{h \cdot c}{\lambda} \quad (3.13)$$

where  $h$  is Planck's constant and  $c$  is the speed of light. Using the previous relationships, the formula for the quantum efficiency  $\eta$  becomes

$$\eta = \frac{g \cdot S \cdot h \cdot c}{E_\lambda \cdot A_{pixel} \cdot T_{int} \cdot \lambda} \quad (3.14)$$



### 3.6.2. Experiment

For quantum efficiency measurements between 400nm and 1100nm a broadband light source (halogen lamp) is focused on the input slit of a monochromator. A bandwidth of 10 Angstrom is selected. The wavelength is scanned in 10-angstrom steps. The imager and a calibrated photodetector are simultaneously coupled to the output ports of the integrating sphere. Because the light level and the sensitivity of the detector vary over the spectrum, convenient integration times are selected for each wavelength for obtaining signals within the linear region of the imager (10-40% of the full well capacity). The wavelength and exposure times are selected manually. The photodetector output is recorded for each wavelength. After that the measurement is automatic, eight different rows of the imager are fully readout and stored. In the end, the row average is used to calculate the mean number of carriers in the potential wells for each type of pixel. Using (3.14) quantum efficiency is calculated and plotted.

For quantum efficiency measurements between 300nm and 400nm the halogen light source is replaced with a stable deuterium lamp. Due to the extremely low light level the integrating sphere is removed. During this measurement, the photodetector plane and the imager plane must alternatively be inserted exactly in the same place in space, far enough from the monochromator, where there is a good uniformity of irradiance. This is done by sliding both the imager and the photodiode on a rail perpendicular to the output light beam from the monochromator (Figure 3.8). The array is thermoelectrically cooled at  $-30^{\circ}\text{C}$ . The readout speed is 16.7 kHz.

### 3.6.3. Experimental setup

The schematics of the setups used to measure quantum efficiency at different wavelength ranges are shown in Figure 3.7. Figure 3.8 contains a photograph of the setup.

An *EG&G model 555-61A* monochromator with an *EG&G model 555-62* filter wheel and an *EG&G model 550-1* radiometer/photometer were used. An *Ealing* halogen source powered by a digital power supply and an *Oriel* deuterium lamp were employed.

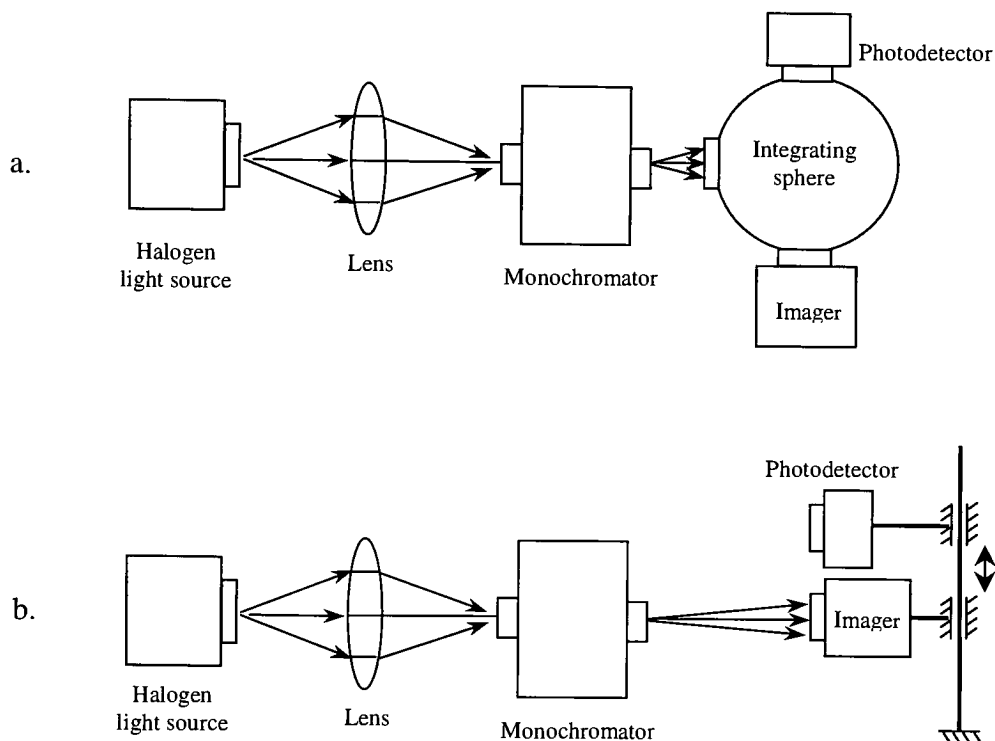


Figure 3.7 Setup for measuring the quantum efficiency for the APCID imager in the wavelength range of 400nm to 1100nm (a) and 300nm to 400nm (b)

The integrating sphere was a 6" diameter *Labsphere*. A 16-bit *Analogic ADC4325* A/D converter and a *National Instruments AT-DIO-32F* card were used for data acquisition.

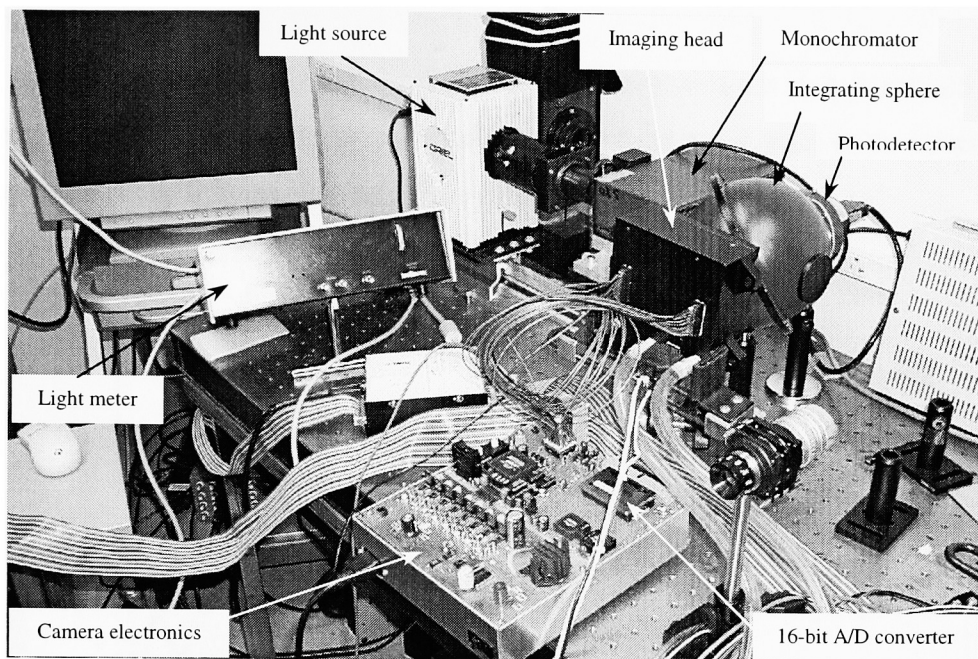


Figure 3.8 A photograph of the setup used for quantum efficiency measurements

### 3.6.4. Results and discussion

Figure 3.10 is a multiple plot showing the spectral quantum efficiency for different types of pixels. Individual quantum efficiency plots are found in Figure 3.19. The values are lower than expected in a device of this type.

An important observation to mention here is that the photogates were purposely placed in an N-well where the concentration of the donor impurities is few orders of magnitude higher than in the native epitaxial silicon. This was done for safety reasons (see section 2.1.) since at the time the design was done a dedicated AP-CID process was not available.

Lower doping in the imaging area would result in a significant increase of quantum efficiency.

Another observation is that the quantum efficiency does not drop too much in blue and near UV, which makes the array suitable for work in that region of the spectrum in applications such as lithography and UV inspection.

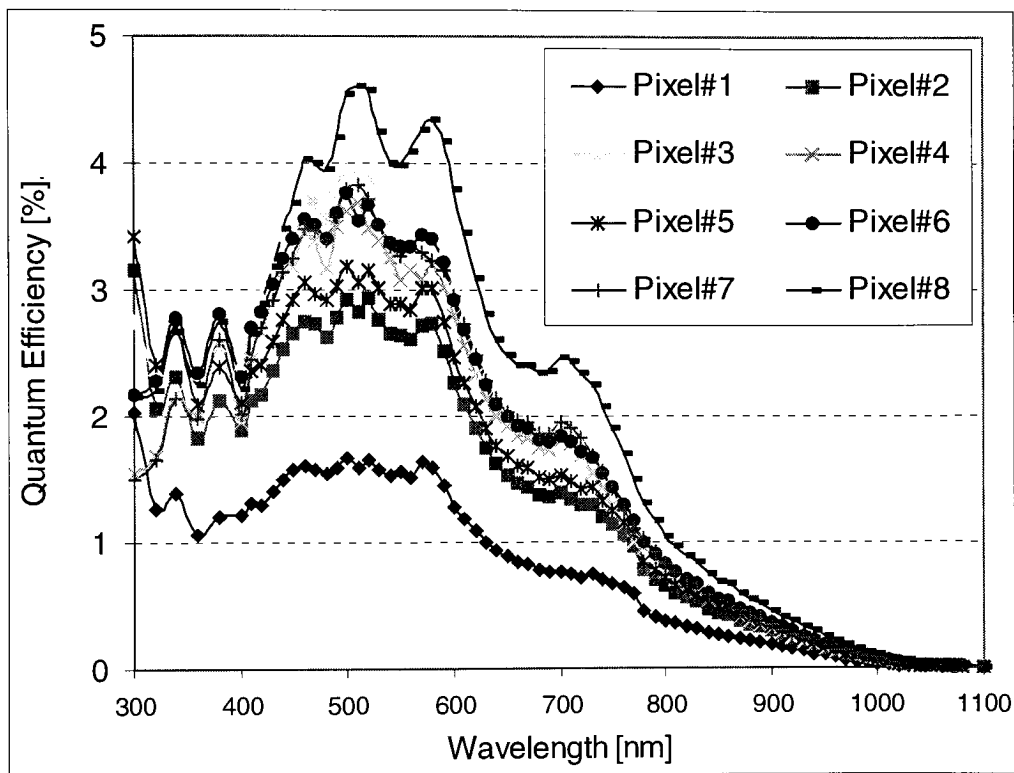


Figure 3.9 Quantum efficiency plots for various pixel configurations

A remarkable thing is that some of the pixels actually exhibit maximum spectral quantum efficiency at a wavelength of 300nm.

The quantum efficiency in red and near infrared drops significantly. The array is built on a relatively thin epitaxial layer (15  $\mu\text{m}$ ) which increases the chance that minority carriers generated deeper in the silicon to be swept into the substrate by the built in field

across the epi-substrate junction (section 1.3.2). To improve the infrared sensitivity, the thickness of the epitaxial layer upon which these arrays are built have to be increased (section 1.2.1) by 50-100%. This fact however would negatively impact the modulation transfer function of the pixel since charge carriers generated in one pixel would have a greater chance to drift to neighboring pixels.

A summary of the quantum efficiency measurement is presented in the table below.

Wavelength	Pixel#1	Pixel#2	Pixel#3	Pixel#4	Pixel#5	Pixel#6	Pixel#7	Pixel#8
300nm	2.03	3.15	2.75	1.55	3.43	2.17	1.51	2.15
520nm	1.66	2.94	3.89	3.48	3.15	3.68	3.71	4.58
800nm	0.38	0.65	0.85	0.76	0.71	0.83	0.84	1.05

Table 3.2 Percentage quantum efficiency values at three different wavelengths

## 3.7. Dark currents

### 3.7.1. Experiment

Dark current is due to the thermal generation of free charge carriers around defects within the semiconductor or at the semiconductor-oxide interface. Having typical values around hundreds of pA/cm<sup>2</sup>, at room temperature, the value of the dark current doubles for every 8 K increase in temperature<sup>24</sup>.

The dark current measurement is performed at several temperatures. The imager is cleared from charge and the output signal is monitored for various integration times. For a precise measurement at a given temperature, several exposure times have to be selected for which the average output lays within the linear region of the characteristic curve.

Using the previously measured gain (section 3.3), a graph of the collected charge versus the exposure (time in the dark) is plotted.

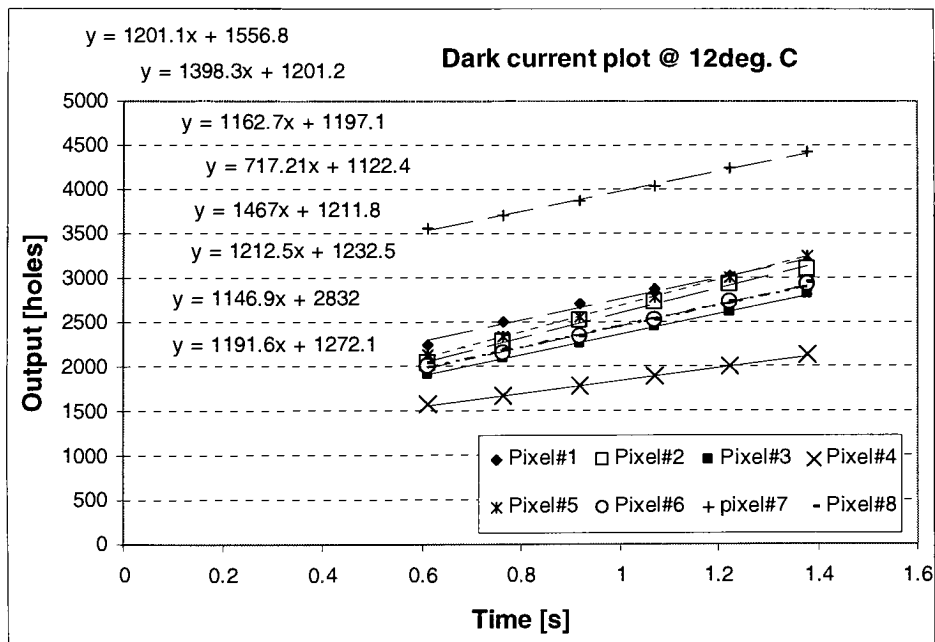


Figure 3.10 Example of dark current (slope) estimation at 12°C

The slope of a linear fit of the points in this graph gives the dark current within a pixel (see the graph above). Dividing this current with the pixel area results in the dark current density (nA/cm<sup>2</sup>) at a given temperature. A variation of the dark current density with the temperature is plotted.

### 3.7.2. Results and discussion

The dependence of dark current versus temperature is plotted in the graphs below. About 200nA/second at room temperature and an increase of an octave for each 7.9°C was observed. These are typical numbers for surface channel CID processes. The dark current performance can be improved by running the array at low temperatures.

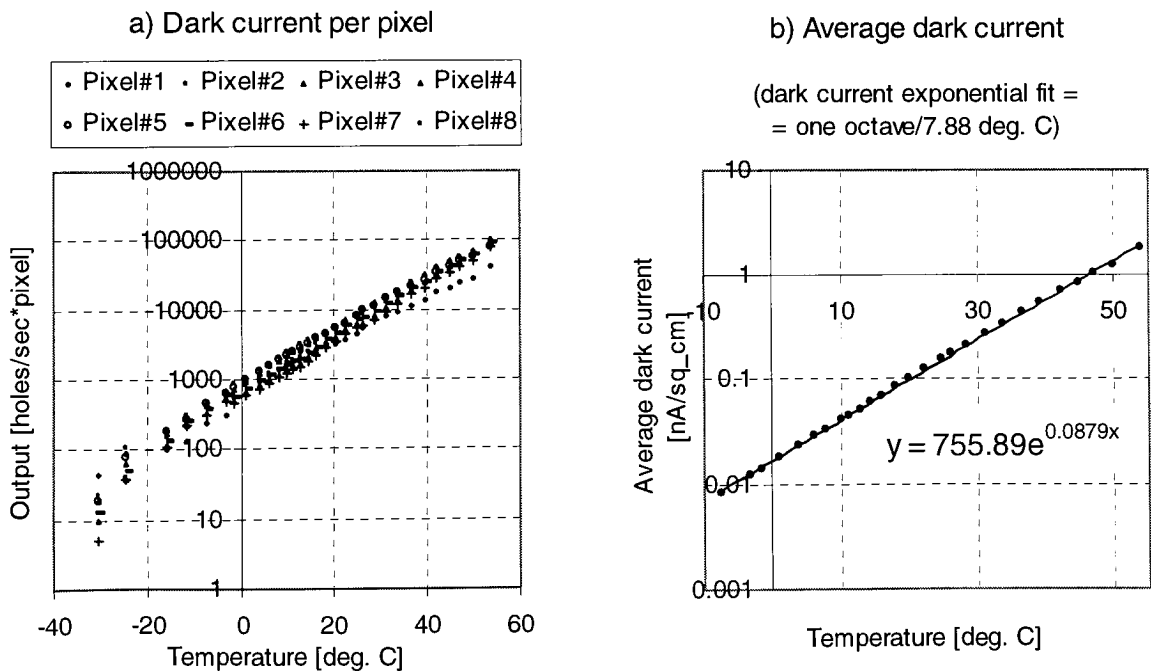


Figure 3.11 Dark current plots at various temperatures: for each individual pixel (a), an average per surface (b)

An interesting aspect is calculating the temperature at which the dark current shot noise is below the readout noise floor of the imager. Let's assume an integration time of 1 second and a minimum readout noise of 5 electrons. Assuming a Poisson statistics, the dark current producing that value of shot noise is the value of the noise raised at power two. In our case, the temperature at which the dark current is below 25 electrons/pixel is – 30°C (see Figure 3.11).

Another interesting aspect is calculating the time at which the dark current noise is equal to the readout floor noise at room temperature. From Figure 3.11 that time is 25ms which considering a negligible integration time and 400 pixels/frame corresponds to 16kHz. So there is actually possible to approach a good precision in measuring the gain/noise at room temperature if the frequency of operation exceeds 16kHz.

In order to do a comparison between pixels of the effect of the dark current on the imaging performance the ratio quantum efficiency over dark current is calculated at a given wavelength. The ratio will be called dark current merit factor.

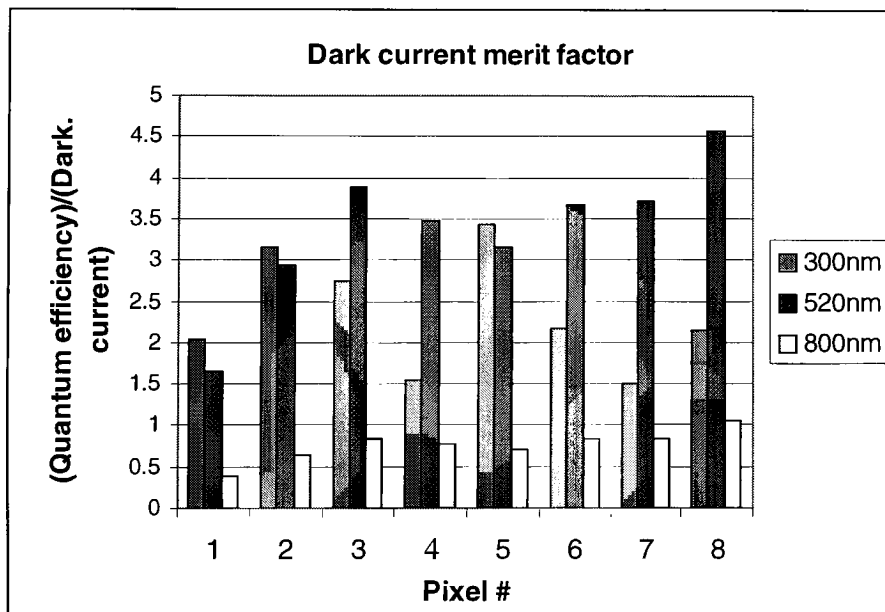


Figure 3.12 Dark current merit factor



## 3.8. Fixed pattern noise (FPN) and shading measurement

### 3.8.1. Background

Exposing an imaging array to a perfectly uniform gray scene, the image output will not be uniform. Generally speaking, FPN of an imaging array represents the systematic component of the pixel-to-pixel variation in output signal under uniform illumination. The image of an arbitrary scene and the fixed pattern noise will overlap at the output of the imager. Visually one has the impression of viewing the scene through a stained glass. This is a serious drawback especially in active pixel sensors, and is mainly caused by pixel to pixel variations in the pixel parameters. The CDS readout technique reduces the FPN induced by variations in the threshold of the preamplifier. FPN can be defined in several ways. In this case we will consider it as the spatial (pixel to pixel) root mean square error about the frame average while the imager is uniformly illuminated. FPN having low spatial frequencies (spatial periods comparable to the image size) is called shading. The human eye can tolerate significant more shading than FPN.

For measuring the FPN the imager is uniformly illuminated. A low-pass filtered version of the image (LPFI) is subtracted from the original image in order to eliminate shading. The filtering is applied on the output data by using a low-pass filtering kernel of size 20 (each pixel in the low-pass filtered image is the average of 20 neighboring pixels). On this new image an RMS deviation about the frame average is calculated and divided by the frame average for the maximum output image.

$$FPN_{r.m.s.} = \frac{\text{StandardDeviation}(\text{Image} - \text{LPFI})}{\text{MaxAverageImage}} \quad (3.1)$$

A similar formula is used for shading:

$$Shading_{r.m.s.} = \frac{\text{StandardDeviation}(\text{LowPassFilteredImage} - \text{AverageLPFI})}{\text{MaxAverageImage}} \quad (3.15)$$

An important remark here is that MaxAverageImage in the above formulas represents the average of the image with the higher exposure in the series (explanations are in the next section).

### 3.8.2. Experiment

The imager is being uniformly illuminated with 10 different levels of exposure from 0% to 90% of the saturation level. The procedure is repeated 16 times and 10 average frames are computed for each light level. For any of these frames each pixel value will be the average of 16 pixel values taken at the same light level so that the effect of temporal noise is minimized.

For each average frame a low-pass-filtered average frame is computed and FPN and shading are calculated using the formulas in the previous section. The low pass filtered image (LPFI) is obtained by using a low pass kernel of size 20.

### 3.8.3. Results and discussion

Figure 3.13 shows an example of FPN and shading plots. A full set of plots is found in section 3.11.4 and section 3.11.5.

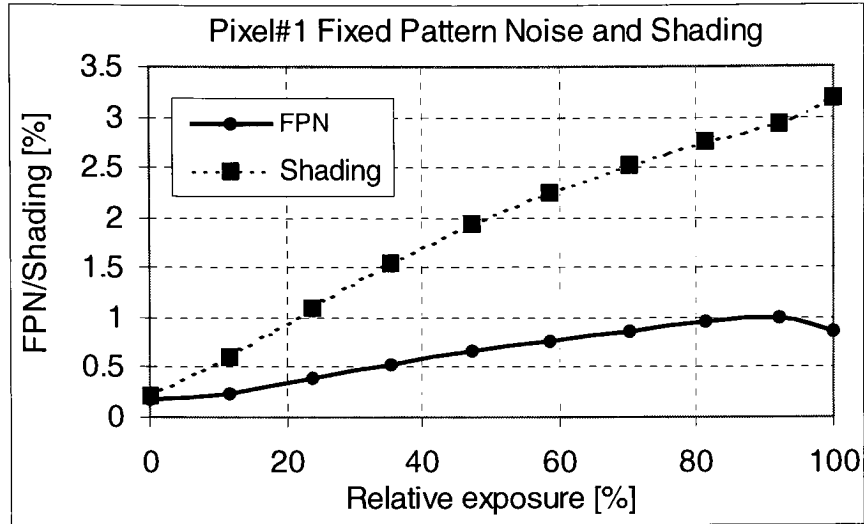


Figure 3.13 Fixed pattern noise and shading for pixel#2

From these plots one can see that the shading is typically higher than FPN for any given pixel configuration. There is a tendency for pixels with larger photogate area to exhibit a smaller FPN value in the dark than the other pixels. This is very important since in the dark the value of the shot noise is small and the fixed pattern noise is more visible.

It is interesting to mention that both FPN and shading plots have a small region beyond 80% of the exposure range for which the derivative of the curves turns negative. This is because the imager begins to saturate and the incremental slope in transfer characteristic becomes smaller. As a consequence both the FPN and shading will decrease.

## **3.9. Nonlinearity fixed pattern noise (NLFPN) measurement**

### **3.9.1. Background**

The fixed pattern noise measured for various types of pixels has quite large values. During the measurement it was observed that both FPN and shading are affected by biasing conditions, and there is an obvious effect of the pixel geometry on both parameters. Besides obvious charge transfer efficiency in pixels with very long gates, which make the FPN very dependent on biasing conditions, it seems that this parameter is mostly dependent on the pixel size and the manufacturing process. The larger the pixels the lower the pixel to pixel relative parameter variations. For our process, at 27mm pixel size, it is hard to get lower than 1% r.m.s. FPN.

A useful metric for characterizing the ability of the imager to be corrected for FPN, is the nonlinearity fixed pattern noise NLFPN. We define NLFPN as the fixed pattern noise in the nonlinearity for each individual pixel across the array.

### **3.9.2. Experiment**

The imager is being uniformly illuminated with 10 different levels of exposure from 0% to 90% of the saturation level. The procedure is repeated 16 times and 10 average frames are computed for each light level. For any of these frames each pixel value will be the average of 16 pixel values taken at the same light level so that the effect of temporal noise is minimized.

For each individual pixel a 10-point transfer characteristic is plotted and a linear fit calculated. Nonlinearity is plotted across the frame. The standard deviation of this nonlinearity function represents the nonlinearity fixed pattern noise.

The highest exposure data is then dropped from the calculation and another NLFPN is calculated for a smaller fraction of the maximum input range. Again the second brightest frame is dropped and another value for NLFPN is calculated and so on until only three points remain.

Figure 3.14 shows the NLFPN, FPN and nonlinearity for pixel#2. It is important to mention that the nonlinearity was previously measured on an average frame basis. In this section, nonlinearity is measured differently as the square root average of the nonlinearity values for every pixel in a frame. The results vary slightly due to pixel variations.

A full set of NLFPN plots is available in section 3.11.6.

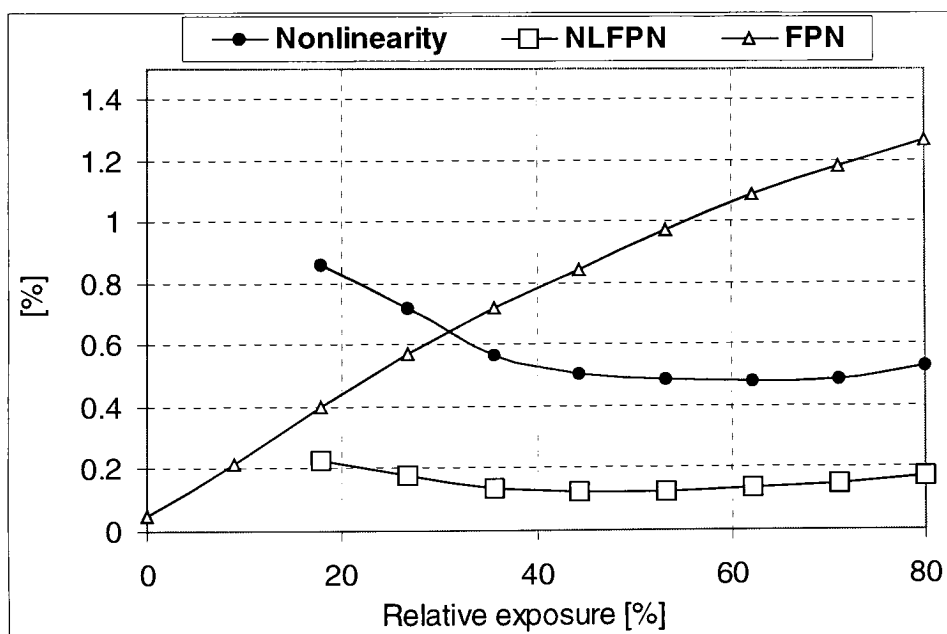


Figure 3.14 Nonlinearity, NLFPN and FPN plotted for various fractions of the maximum input range.

### 3.10. Preamplifier characterization

In order to assess the pixel preamplifier performance, the readout clocking of the 388x16 AP-CID array was modified. Selecting one of the columns corresponding to pixel#2, all the sensing gates were clamped (through the reset transistor) to the *reset drain bus*. Now the whole column is progressively readout for different *reset drain bus* voltages. This way all the preamplifiers along that column can be characterized in terms of nonlinearity, temporal noise, fixed pattern noise and voltage gain.

Table 3.3 contains average values for the pixel preamplifier parameters measured along a whole column for pixel#2 array. ***The size of the preamplifier is the same for all the pixel configurations*** so the data was extrapolated to the rest of the pixels. The asterisk signifies the fact that CDS was not used while measuring this particular noise. A low pass filter kernel was employed to remove very low frequency components from the data. The value of this noise is referenced at the output of the preamplifier.

	Input voltage range	Output voltage range	Voltage gain	Overall output temporal noise*
Pixel#1	271 mV	197 mV	0.729	40-50 $\mu$ V
Pixel#2	542 mV	395 mV	0.729	40-50 $\mu$ V
Pixel#3	948 mV	691 mV	0.729	40-50 $\mu$ V
Pixel#4	1332 mV	971 mV	0.729	40-50 $\mu$ V
Pixel#5	339 mV	247 mV	0.729	40-50 $\mu$ V
Pixel#6	339 mV	247 mV	0.729	40-50 $\mu$ V
Pixel#7	677 mV	494 mV	0.729	40-50 $\mu$ V
Pixel#8	677 mV	494 mV	0.729	40-50 $\mu$ V

Table 3.3 Measured pixel preamplifier parameters at  $-15^{\circ}\text{C}$ .

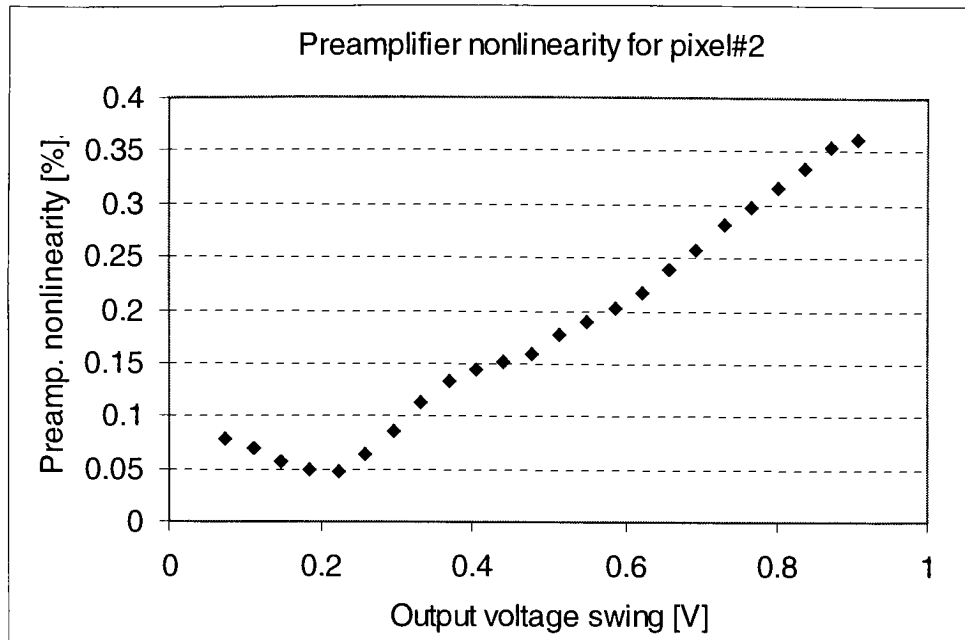


Figure 3.15 Variation of nonlinearity for the pixel preamplifier

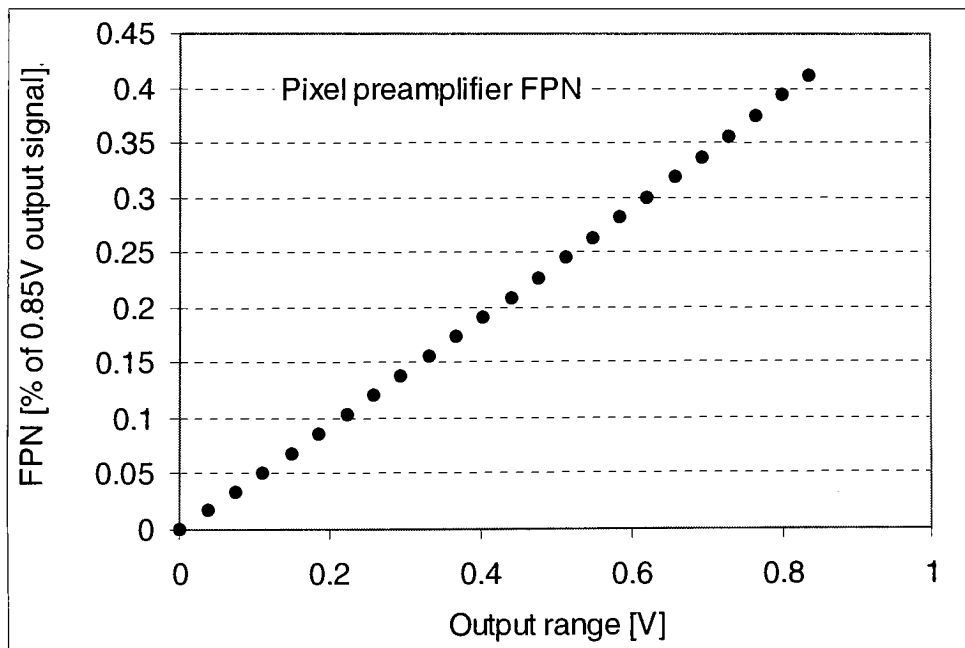


Figure 3.16 Pixel preamplifier FPN

### **3.11. Experimental results appendix**

The present section contains results, in graph form, of the experiments described in this chapter. The section can be used simply as a record for the data collected from each different pixel type during various measurements. The section does not contain any analysis or conclusions relative to the data presented.



### 3.11.1. Transfer characteristic curves

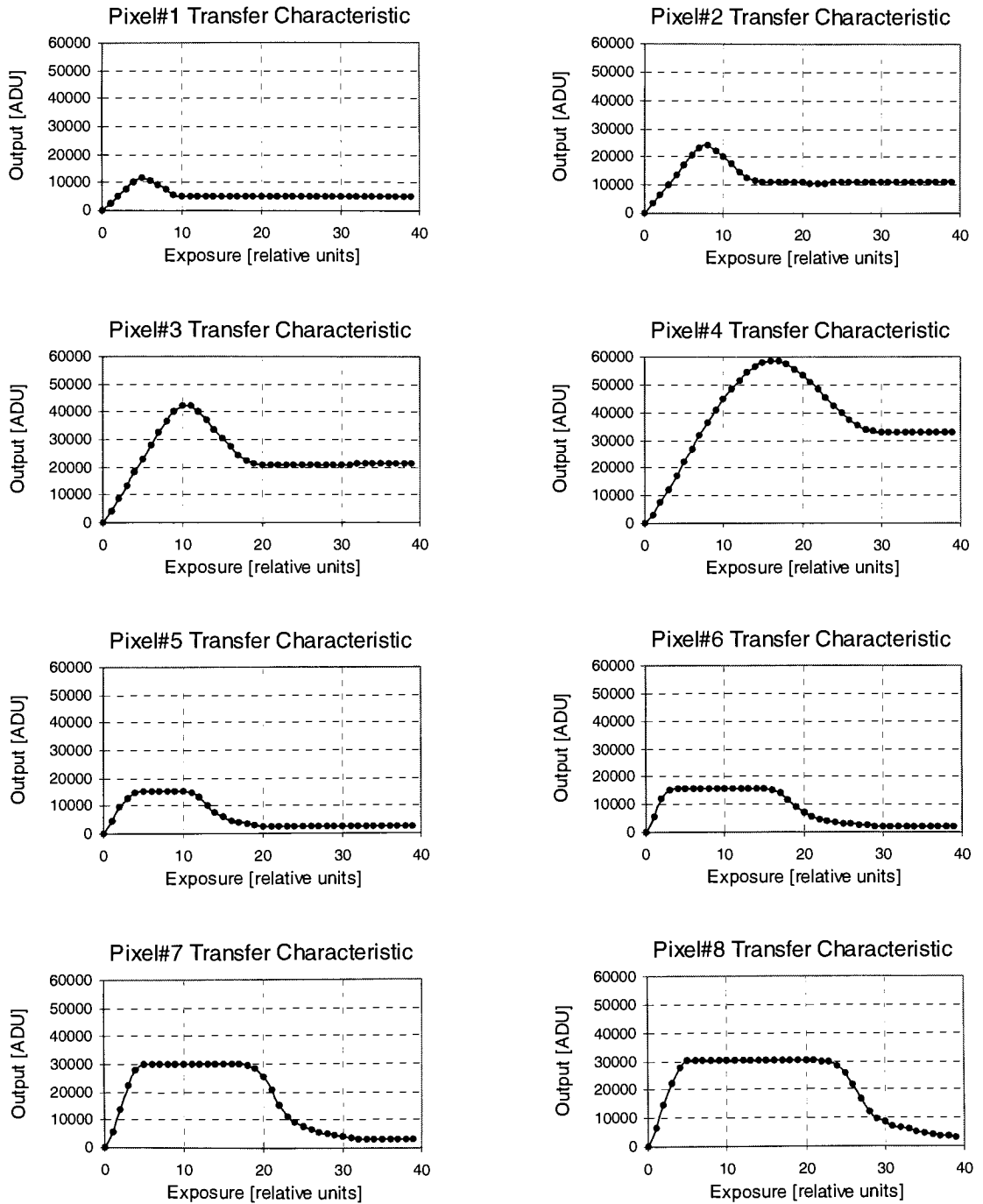


Figure 3.17 Transfer characteristic curves for different pixel architectures

### 3.11.2. Mean-variance plots

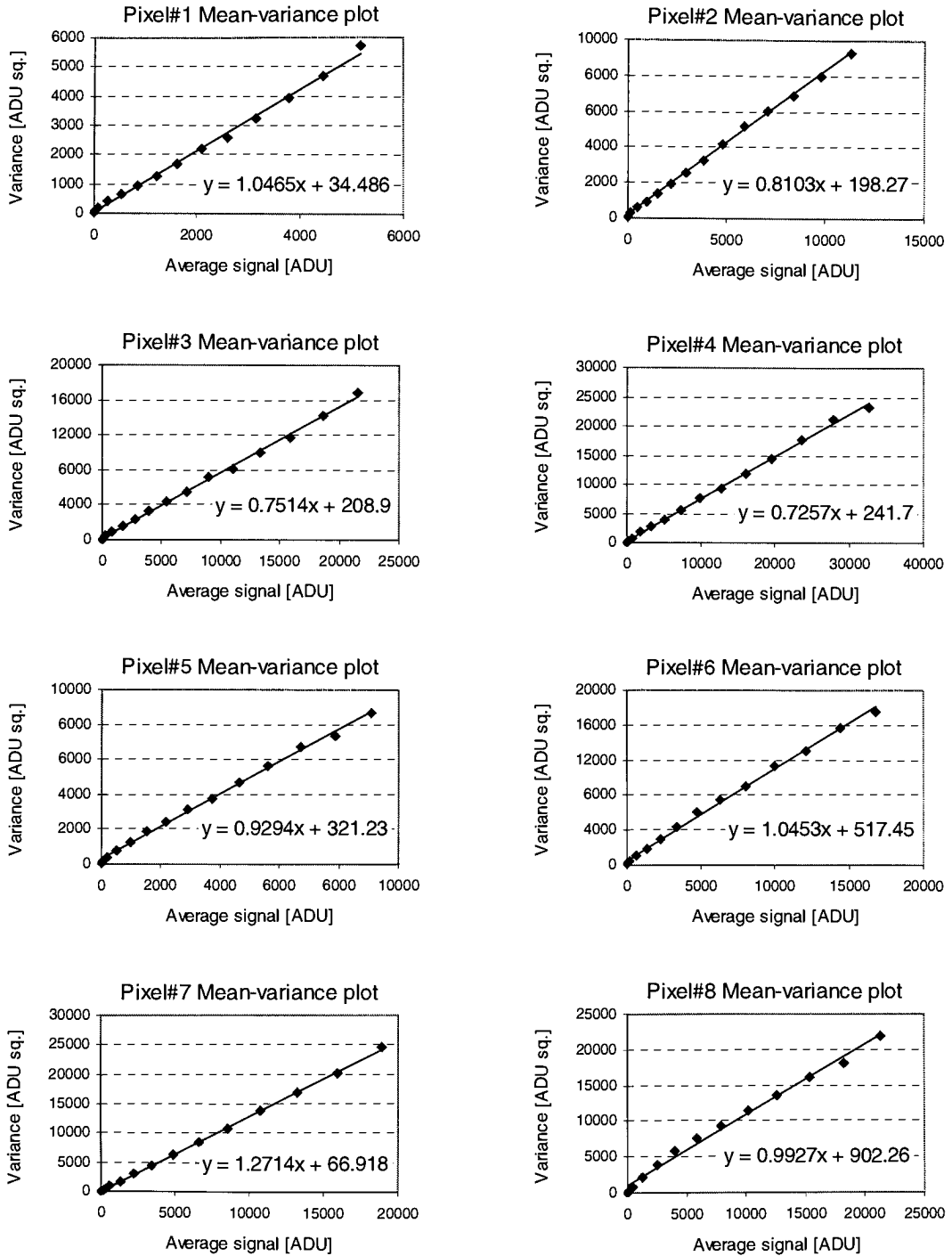


Figure 3.18 Mean-variance plots for different pixel types.

### 3.11.3. Quantum efficiency plots

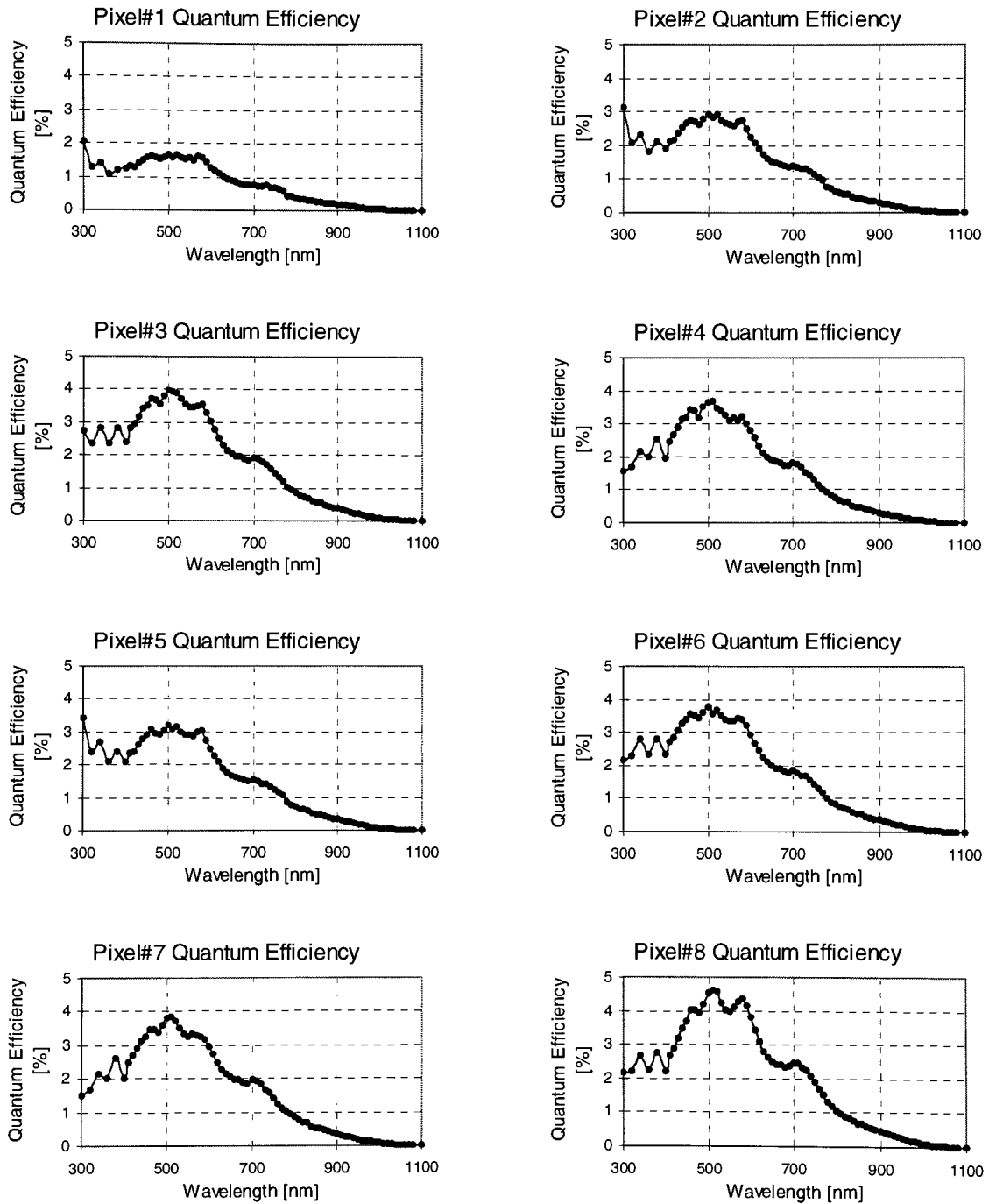


Figure 3.19 Quantum efficiency plots for different pixel parameters

### 3.11.4. FPN Results

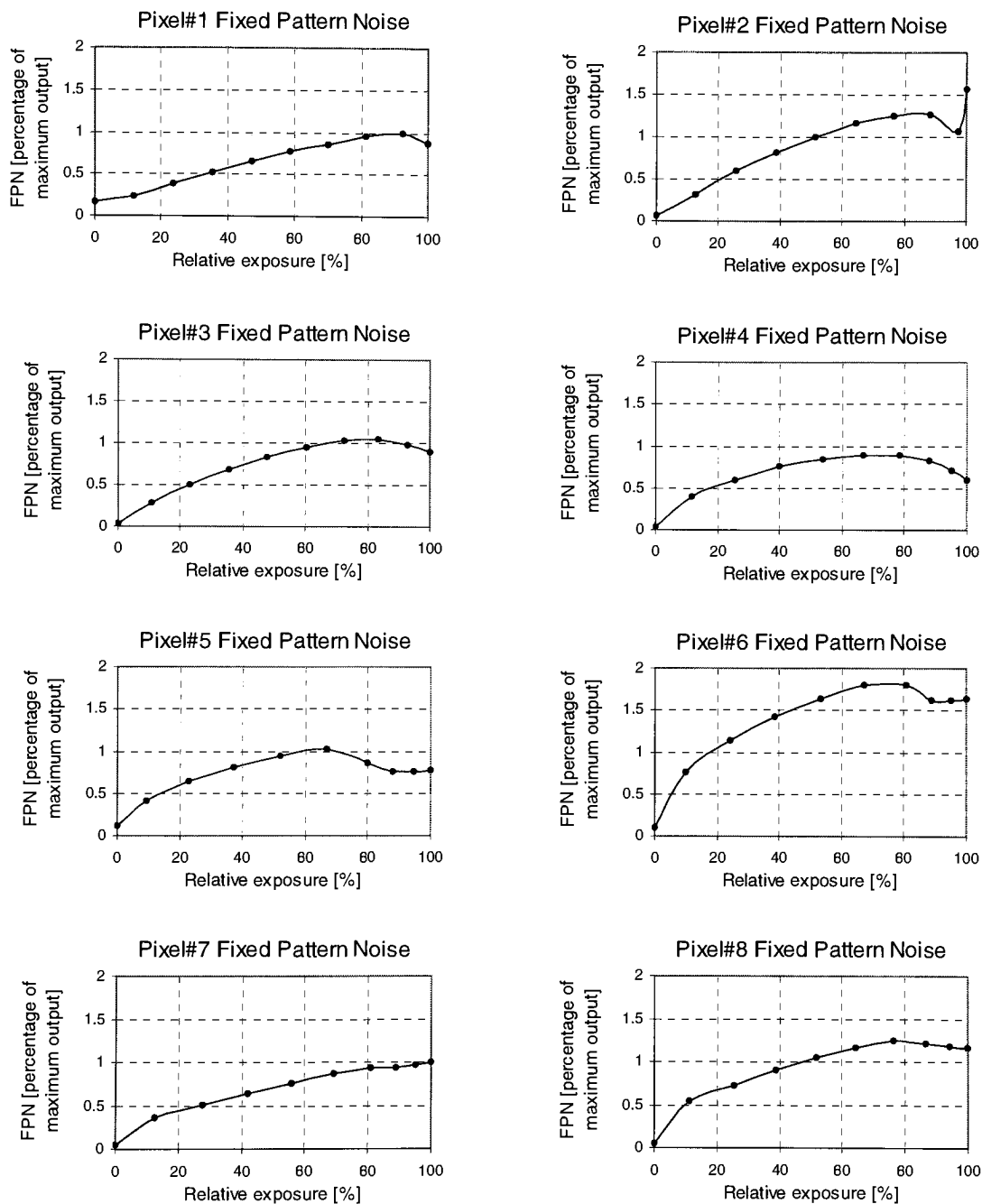


Figure 3.20 Fixed pattern noise results for various pixel architectures. The relative exposure means percentage of the exposure level at saturation for a particular pixel

### 3.11.5. Shading results

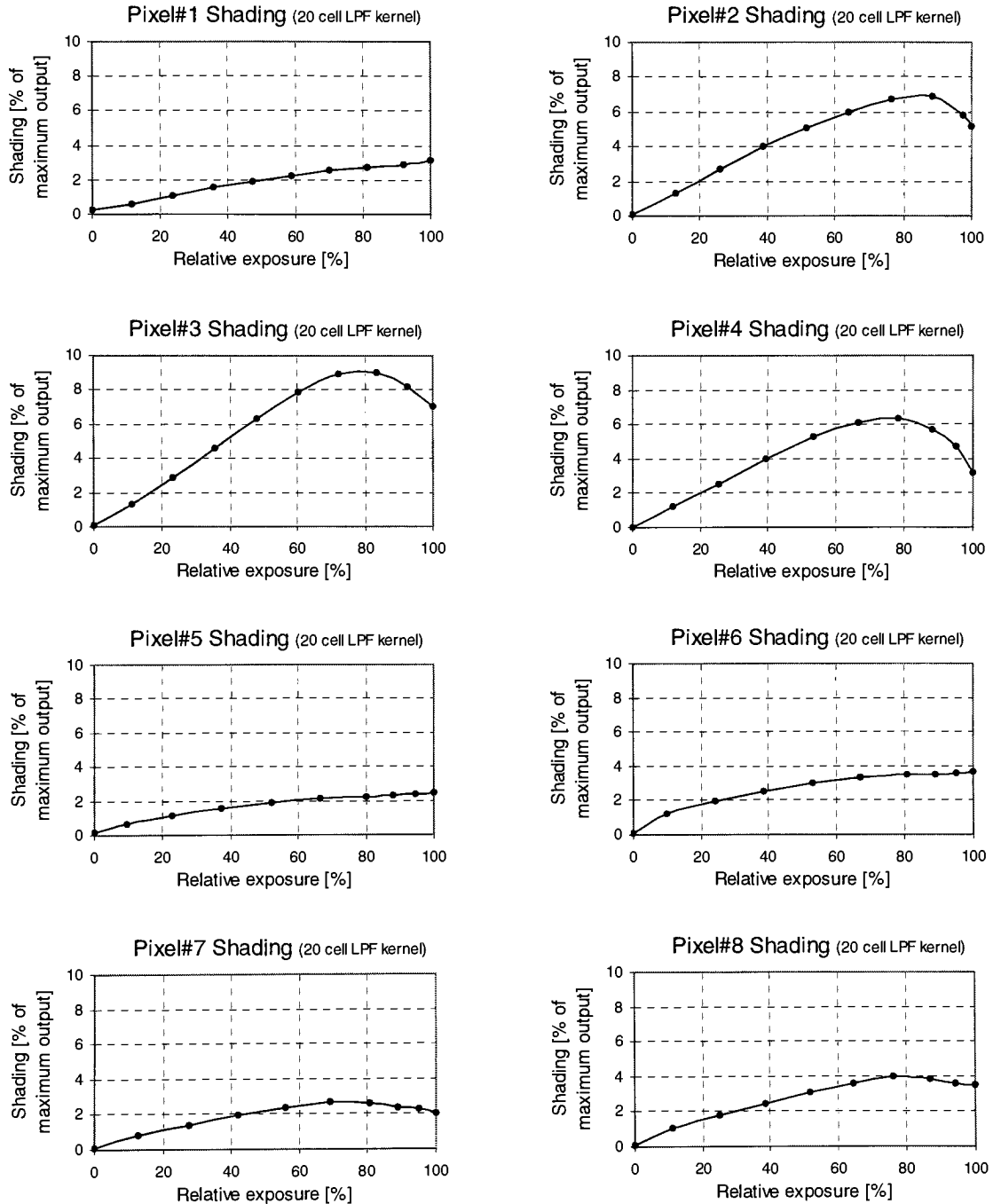


Figure 3.21 Shading results for various pixel architectures. The relative exposure means percentage of the exposure level at saturation for a particular pixel

### 3.11.6. NLFPN results

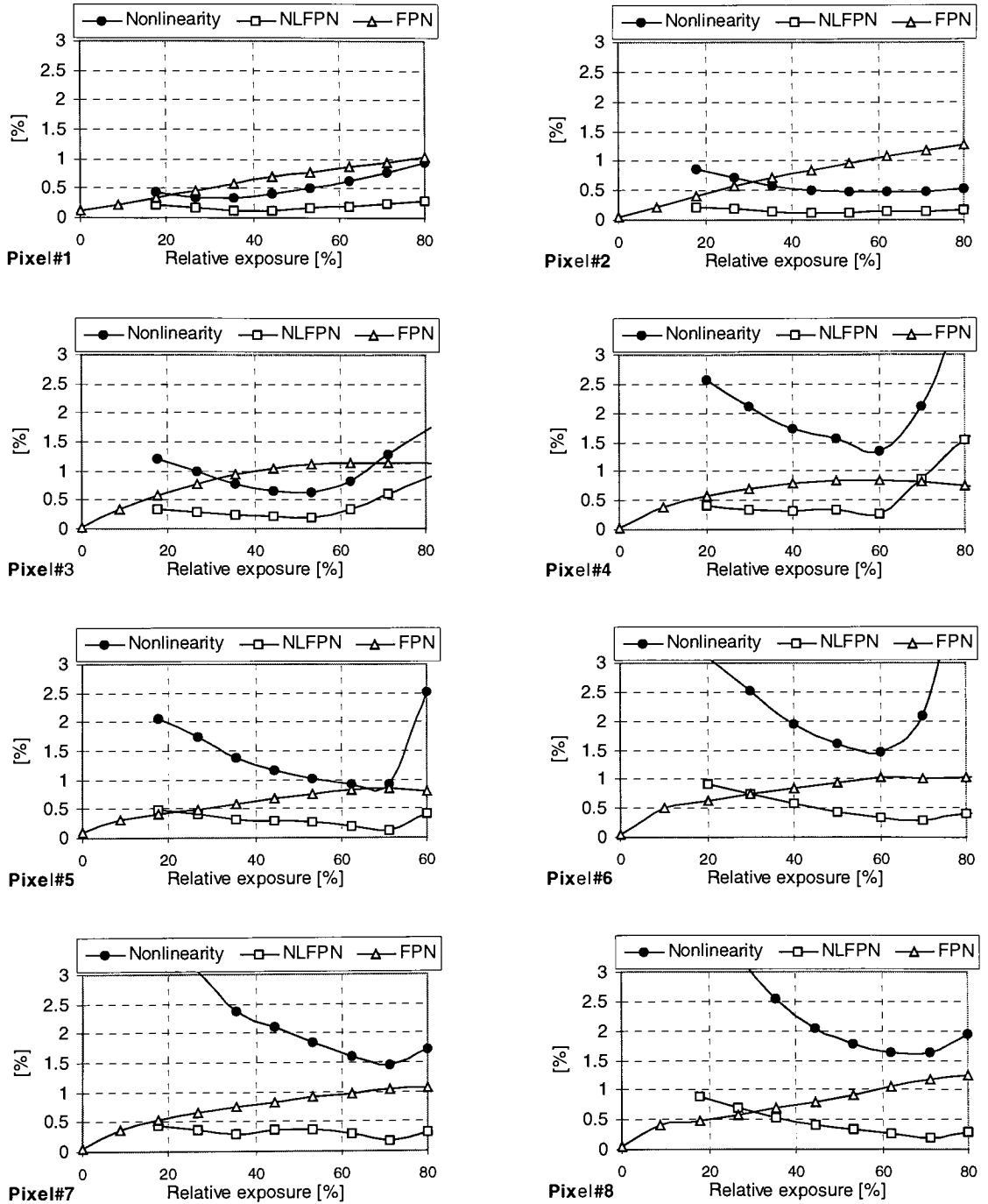


Figure 3.22 Nonlinearity, nonlinearity fixed pattern noise, and fixed pattern noise

# **Chapter 4. Performance analysis and improvement**

## **4.1. Transfer characteristic curve (TCC)**

Looking at the TCC curves in section 3.11.1 we can see the following differences between pixel configurations:

- Different slopes in the linear region
- Different output level at saturation
- Different behavior of the TCC in the saturation region

The above differences will be analyzed in the following section.

### **4.1.1. Pixel sensitivity and saturation level**

The sensitivity of the pixel could be expressed as the slope of the transfer characteristic curve in the linear region (region A and B regions in Figure 4.3). It represents the ratio between the output signal and the amount of exposure necessary to obtain that output level. For 388x16 Orbit AP-CID, since the gain doesn't vary much with the pixel architecture, sensitivity is proportional to quantum efficiency for a certain wavelength.

Figure 4.1 shows the sensitivity and quantum efficiency in red light for various pixel types. As a general tendency the larger the photogate areas the larger the sensitivity in long wavelength radiation.

The saturation level is the maximum signal level achievable with a certain pixel.

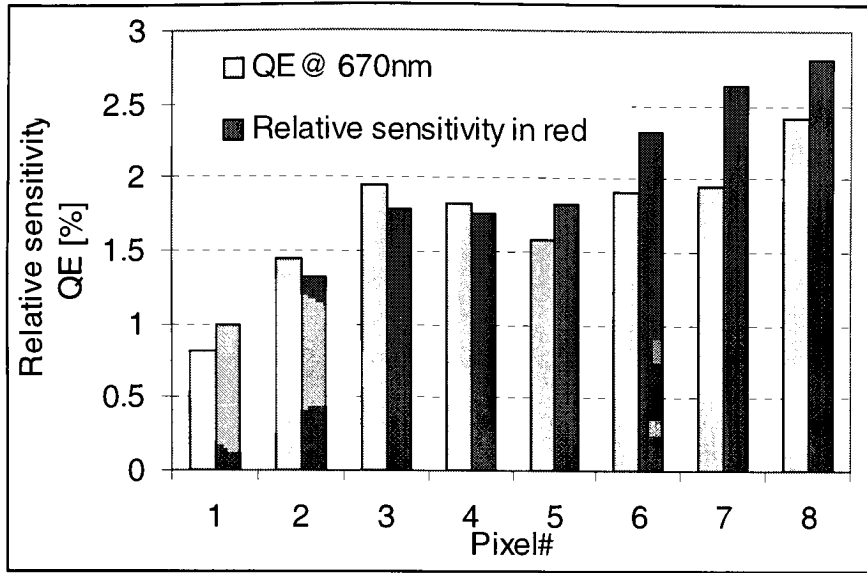


Figure 4.1 Relative sensitivity in red light for different pixel configurations

A relative value of the maximum saturation output level is plotted in Figure 4.2 together with the sensing gate area for various pixel configurations.

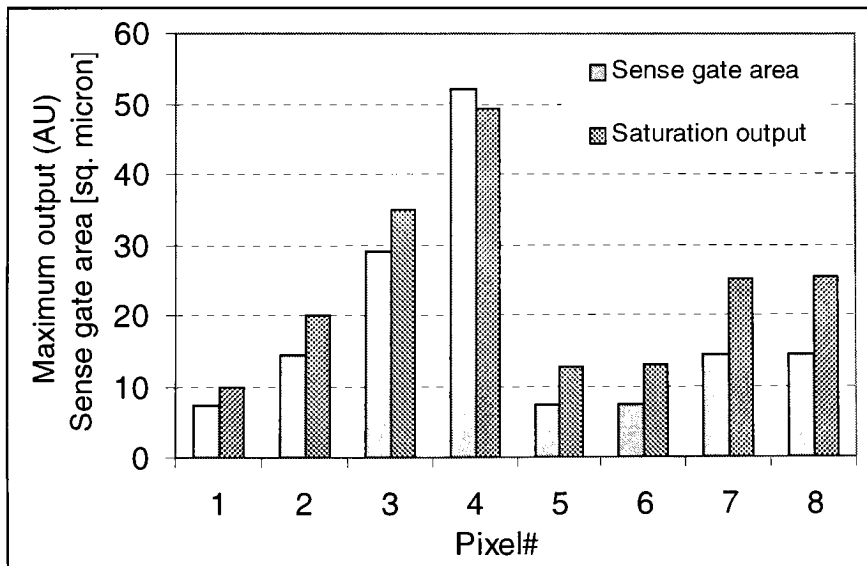


Figure 4.2 Maximum output and sense gate area for various pixel configurations



The graph shows a strong correlation between these two parameters, which confirms the fact that the larger the sensing gate capacitance the less charge sharing will occur between the sense electrode and the parasitic capacitances associated, hence the larger the maximum output signal.

#### 4.1.2. Gain regions of the transfer characteristic curve

A particular aspect, characteristic to three-electrode CID pixels, is the fact that the TC curve doesn't remain flat after saturation but starts falling off after a certain exposure interval from the saturation point, depending on the pixel architecture and the electrode bias voltage. The camera starts exhibiting a negative gain, in which the output level from bright pixels can be lower than the output from dimmer pixels. It is a parasitic effect and means of controlling it will be suggested.

Figure 4.3 shows seven different gain regions of the TCC for a pixel having the storage gate larger than the sensing gate (pixel#7). The shape of the TCC is analyzed below. This is a first order analysis and for most of it, a very simple model is used.

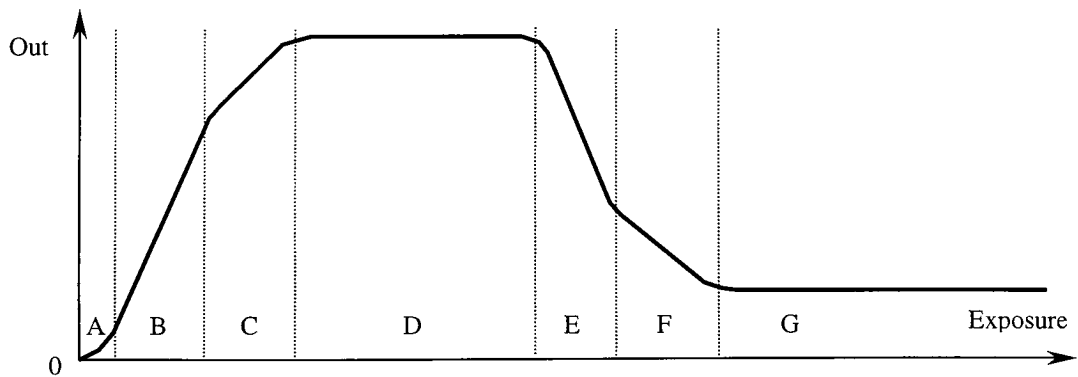


Figure 4.3 Transfer characteristic curve of a generic 3-electrode AP-CID having storage gate larger than sensing gate, exhibiting seven different gain regions

The sensing gate is assumed isolated hence there is no capacitive coupling between this gate and any other element in the pixel (except the electric charge in the corresponding potential well). This assumption is not true at all in any real pixel architecture active or passive, where the sensing gate shares charge with parasitic capacitances in the pixel. These parasitic capacitances include the gate on the preamplifier and the drain/source of the preset transistor.

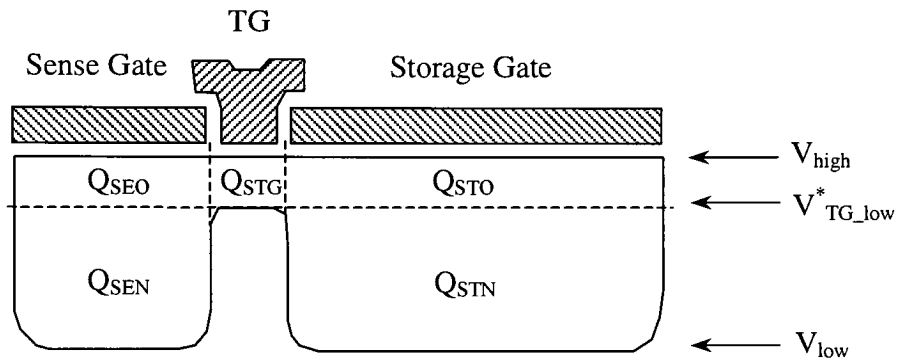


Figure 4.4 A potential wells diagram of a three electrode CID pixel. Generic names for five significant volumes within potential wells are indicated. The notations on the right side of a certain well level represent the photogate voltages for which the bottom of the potential well reaches the respective level.

Another approximation is that 100% of the charge from a potential well is transferred under the other wells while the first is collapsed.

If there is not enough room in the potential wells during a charge operation, the excess of the charge is injected in the substrate (disappears) after the potential wells are filled up. The very last statement is true in real CID's.

Another assumption is that the threshold voltage for all the photogates is the same.

Potential well volume (charge)	Shorthand notation	Value
Normal sense electrode charge	$Q_{SEN}$	$C_{sense}A_{sense}(V_{TG\_low}^* - V_{low})$
Overflow sense electrode charge	$Q_{SEO}$	$C_{sense}A_{sense}(V_{high} - V_{TG\_low}^*)$
Transfer gate charge	$Q_{STG}$	$C_{TG}A_{TG}(V_{high} - V_{TG\_low})$
Normal storage electrode charge	$Q_{STN}$	$C_{sense}A_{store}(V_{TG\_low}^* - V_{low})$
Overflow storage electrode charge	$Q_{STO}$	$C_{sense}A_{store}(V_{high} - V_{TG\_low}^*)$

Table 4.1 Significant potential well volumes: notations and values

The epitaxial layer voltage is set at one threshold voltage above  $V_{high}$ . As a consequence as far as charge is concerned, the potential well volume under a certain gate is  $C_{gate}A_{gate}(V_{high} - V_{gate})$  while that gate is set at a potential  $V_{gate}$  (see bibliography ref. 15).

Table 4.1 shows the names and values for five significant potential well volumes.  $C_{sense}$ ,  $C_{store}$  and  $C_{TG}$  are the capacitances of the corresponding gates per unit area.  $A_{sense}$ ,  $A_{store}$  and  $A_{TG}$  are gate areas.

The storage/sensing are made of poly\_2 and the transfer gate is made of poly\_1. The gate oxide thickness is 560 nm for store/sense photogates, and 225 nm the thickness of the oxide corresponding to for the transfer gate. This means that for the same voltage, the transfer gate will have a deeper potential well than the sense/storage electrodes.

In order to simplify the algebraic calculations we will introduce  $V_{TG\_low}^*$ , which is *the depth of the transfer gate potential well as seen from the sense/store potential wells* while the voltage on the TG is  $V_{TG\_low}$ . The idea is to treat the three-electrode structure as if the same oxide thickness would exist under all electrodes.

In order to find the value of  $V_{TG\_low}^*$  a condition of charge equality has to be written:

$$Q_{TG}(V_{TG\_low}) = Q_{TG}^*(V_{TG\_low}^*) \quad (4.1)$$

$$\text{which means } V_{TG\_low}^* = V_{high} - \frac{C_{TG}}{C_{sense}} \cdot (V_{high} - V_{TG\_low})$$

It is important to mention that  $C_{TG}$  and  $C_{sense}$  are capacitances per unit area.

#### 4.1.2.1. *Very low light level linear region (A)*

In this region, there is very little charge in the potential wells. The transfer characteristic has a convex shape (positive second derivative), which is due to reduced charge transfer speed/efficiency effects. As seen in section 1.2.3 there are three charge transfer mechanisms: thermal diffusion of charge carriers, transfer by self-induced electric fields and transfer by fringing fields. At very low charge level the only fast charge transfer mechanism is by fringing fields<sup>16</sup>. For certain pixel architectures (pixel#1,2) the storage gate is short (3-6μm) while for others the storage gate is longer. There is a general tendency that the nonlinearity of the TCC at low output levels is directly proportional to the length of the storage gate.

Pixel#	Storage gate length [μm]	Nonlinearity @ 30% of input range [%]
1	3	0.6
2	6	1.4
3	12	1.9
4	24	2.4
5	12	1.45
6	24	4.3
7	38	4.7
8	20	4.7

Table 4.2 Nonlinearity at low light levels

Making abstraction of the charge transfer inefficiency, the formula of the TCC in this region will be derived in the next section.

As a conclusion, in order to improve the linearity in this region, the charge transfer efficiency has to be improved by avoiding long and winding photogates or by manufacturing the device in a buried channel technology.

#### 4.1.2.2. *Linear region (B)*

Here the charge accumulated in the sensing well during the phase of light integration is transferred to the storage well during the operation of *back transfer*. During the *forward transfer* phase, all the charge accumulated in the pixel is transferred to the sensing well.

The linear region is as the region of the TCC where the total charge in the wells is smaller than  $Q_{SEN}$ .

$$Q_{total} < Q_{SEN} \quad (4.2)$$

By definition, the quantum efficiency ( $\eta$ ) is the ratio between the number of charge carriers captured in the potential wells of the pixel ( $Q_{total}$ ) and the number of photons falling on the pixel area during the exposure interval (*Exposure*).

$$\eta = \frac{Q_{total}}{Exposure} \quad (4.3)$$

In this case, the idealized charge to voltage conversion is linear, which means after the sense gate is left floating at the  $V_{low}$  potential and the charge  $Q_{total}$  is transferred in the corresponding potential well, the voltage of the sense electrode will rise to the value:

$$V_{sense} = V_{low} + \frac{Q_{total}}{C_{sense} \cdot A_{sense}} \quad (4.4)$$

Combining the previous formulas we obtain the equation of the characteristic curve in the linear region:

$$V_{sense}(Exposure_B) = V_{low} + \frac{Exposure_B \cdot \eta}{C_{sense} \cdot A_{sense}} \quad (4.5)$$

The exposure range for being in the linear region is (using information from Table 4.1):

$$Exposure_B < \frac{C_{sense} \cdot A_{sense} \cdot (V_{TG\_low}^* - V_{low})}{\eta} \quad (4.6)$$

#### 4.1.2.3. *Nonlinear charge-sharing region (C)*

After the total charge in the pixel gets larger than  $Q_{SEN}$  the part of electric charge exceeding that value will be shared between the sensing gate and the transfer gate. Because less charge will end up under the sensing gate now, the incremental gain of the imager will be reduced.

The charge-sharing region is the region of the TCC where the total charge in the wells satisfies the condition:

$$Q_{SEN} < Q_{total} < Q_{SEN} + Q_{SEO} + Q_{TG} \quad (4.7)$$

Let's derive the TCC formula based on the fact that there is the same voltage variation  $\Delta V$  above the  $V_{TG\_low}^*$  level in both the sensing potential well and the transfer gate potential well.

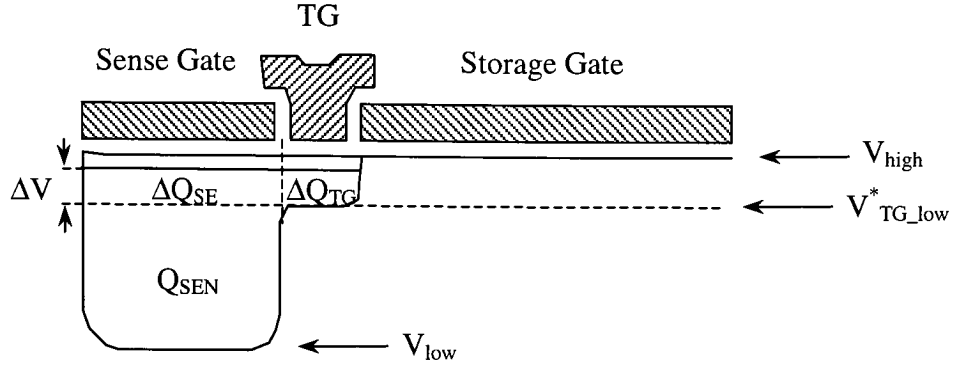


Figure 4.5 A diagram showing the charge sharing process between the transfer potential well and the sense potential well after the storage potential well is collapsed

$$\begin{cases} Q_{total} = \eta \cdot Exposure = Q_{SEN} + \Delta Q_{SE} + \Delta Q_{TG} \\ \Delta V = \frac{\Delta Q_{SE}}{C_{sense} \cdot A_{sense}} = \frac{\Delta Q_{TG}}{C_{TG} \cdot A_{TG}} \end{cases} \quad (4.8)$$

Solving the system of equations (4.8) we obtain the characteristic curve in the charge transfer region:

$$V_{sense}(Exposure_c) = V_{TG\_low}^* + \frac{Exposure_c \cdot \eta - Q_{SEN}}{C_{sense} \cdot A_{sense} + C_{TG} \cdot A_{TG}} \quad (4.9)$$

The exposure range for being in the charge transfer region of TCC is:

$$\begin{aligned} & \frac{C_{sense} \cdot A_{sense} \cdot (V_{TG\_low}^* - V_{low})}{\eta} < Exposure_c < \\ & < \frac{C_{sense} \cdot A_{sense} \cdot (V_{high} - V_{low}) + C_{TG} \cdot A_{TG} \cdot (V_{high} - V_{TG\_low})}{\eta} \end{aligned} \quad (4.10)$$

#### 4.1.2.4. Plateau saturation region (D)

In this region the output of the imager is maximum and constant with exposure. This is because after the sense and TG potential wells are completely filled up with charge from storage well during the phase of forward transfer, the excess of charge in the storage well generated by increasing exposure levels will be injected into the substrate. To the right, the region is bound by the condition that charge starts leaking back into the sensing potential well after the back transfer operation. This happens when the sensing gate is preset at  $V_{low}$  and left floating and marks the beginning of saturation region E.

The plateau saturation region-D is the part of the TCC where the total charge in the wells satisfies the condition:

$$Q_{SEN} + Q_{SEO} + Q_{TG} < Q_{total} < Q_{STN} \quad (4.11)$$

The equation of the characteristic curve in the plateau saturation region-D is a constant and it is the maximum value of the curve in the nonlinear charge-sharing region (C):

$$V_{sense} = V_{high} \quad (4.12)$$

The exposure range for being in the saturation region-D of the TCC is:

$$\begin{aligned} & \frac{C_{sense} \cdot A_{sense} \cdot (V_{high} - V_{low}) + C_{TG} \cdot A_{TG} \cdot (V_{high} - V_{TG\_low})}{\eta} < \\ & < Exposure_D < \frac{C_{store} \cdot A_{store} \cdot (V_{TG\_low}^* - V_{low})}{\eta} \end{aligned} \quad (4.13)$$



#### 4.1.2.5. Steep decline saturation region (E)

In this region the output of the imager drops relatively fast with exposure. The situation is depicted in Figure 4.6. The normal volume ( $Q_{STN}$ ) of the storage potential well is full now and some of the charge leaks back under the sensing gate right after the *back-transfer* operation. As far as the “leak-back” charge brings the potential in the sensing well to a level less than  $V_{TG\_low}^*$ , we are in the region E of the TCC. In this region, the total charge in the wells satisfies the condition:

$$Q_{STN} < Q_{total} < Q_{STN} + Q_{SEN} \quad (4.14)$$

There is plenty of charge in the pixel now to fill up the sensing well after the *forward-transfer* operation. The empty volume “ $Q$ ” in the sensing well after the *back-transfer* and charge *leak-back* determines the output signal in this case. Simple mathematical manipulations render the characteristic curve in the steep decline saturation region-E:

$$V_{sense}(Exposure_E) = V_{high} + (V_{TC\_low}^* - V_{low}) \cdot \frac{A_{store} \cdot C_{store}}{A_{sense} \cdot C_{sense}} - \frac{\eta}{A_{sense} \cdot C_{sense}} \cdot Exposure_E \quad (4.15)$$

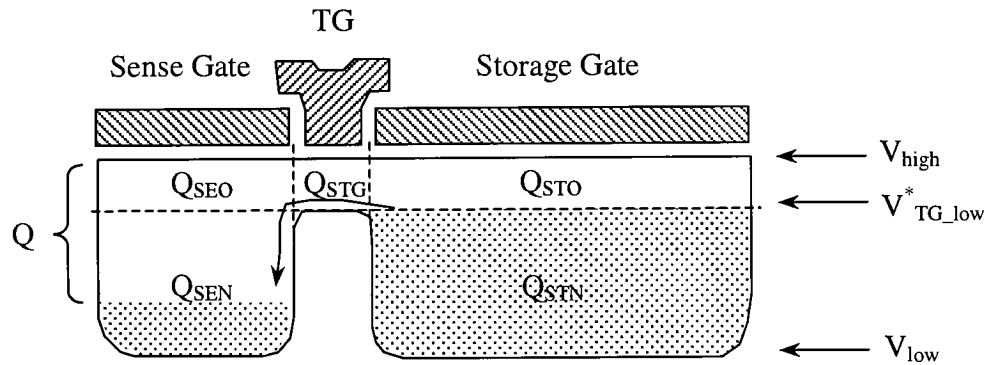


Figure 4.6 Electric charge distribution before the forward transfer for region E of TCC

The exposure condition for being in the steep decline saturation region-E is:

$$\begin{aligned} \frac{C_{store} \cdot A_{store} \cdot (V_{TG\_low}^* - V_{low})}{\eta} < \\ < Exposure_E < \frac{(C_{store} \cdot A_{store} + C_{sense} \cdot A_{sense}) \cdot (V_{TG\_low}^* - V_{low})}{\eta} \end{aligned} \quad (4.16)$$

#### 4.1.2.6. *Shallow decline saturation region (F)*

In this region the situation is similar to the one in region E except that charge sharing between the sense gate and TG starts to manifest. Because of this, the output of the imager still drops with exposure, but slower than in region E.

Here the *back-transfer* will be annihilated by the leak-back since there is so much electric charge in the pixel. For region F, the total charge in the wells satisfies the condition:

$$Q_{STN} + Q_{SEN} < Q_{total} < Q_{STN} + Q_{STO} + Q_{TG} \quad (4.17)$$

Looking at the above relationship we can see that this regime might never happen if  $Q_{SEN}$  is greater or equal than  $Q_{STO} + Q_{TG}$  (for high  $V_{TG\_low}$ ). In this case, region F of the TCC would be missing and region G would follow right after region E.

Let's calculate the incremental charge ( $\Delta Q_{SE}$ ) above the  $V_{TG\_low}^*$  line of the potential well under the sense gate based on the fact that there is the same voltage variation  $\Delta V$  above the  $V_{TG\_low}^*$  level in all the potential wells.

$$\begin{cases} Q_{total} = \eta \cdot Exposure = Q_{SEN} + Q_{STN} + \Delta Q_{SE} + \Delta Q_{TG} + \Delta Q_{ST} \\ \Delta V = \frac{\Delta Q_{SE}}{C_{sense} \cdot A_{sense}} = \frac{\Delta Q_{TG}}{C_{TG} \cdot A_{TG}} = \frac{\Delta Q_{ST}}{C_{store} \cdot A_{store}} \end{cases} \quad (4.18)$$

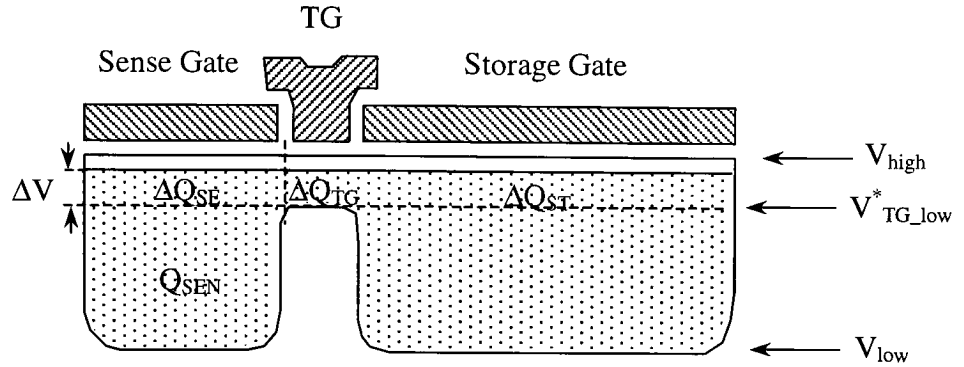


Figure 4.7 Charge diagram for region F before forward transfer

There is a large amount of charge in the pixel while in this region. A back transfer operation will have no effect. A little space in the upper side of the sensing gate will allow charge to completely fill the sensing potential well after the forward transfer operation. That charge (equal to  $Q_{SEO} - \Delta Q_{SE}$ ) will produce a relatively small increase in the sensing gate voltage (output) above the preset level ( $V_{low}$ ) during the forward transfer operation. To find the characteristic curve in this region we can use  $\Delta Q_{SE}$  calculated using the previous system of equations and the following formula:

$$V_{sense} = V_{low} + \frac{(Q_{SEO} - \Delta Q_{SE})}{C_{sense} \cdot A_{sense}} \quad (4.19)$$

Simple mathematical manipulations render the characteristic curve in the shallow decline saturation region-F:

$$V_{sense}(Exposure_F) = V_{low} + V_{high} - V_{TG\_low}^* - \frac{\eta \cdot Exposure_F - (V_{TG\_low}^* - V_{low})(C_{store} \cdot A_{store} + C_{sense} \cdot A_{sense})}{C_{store} \cdot A_{store} + C_{sense} \cdot A_{sense} + C_{TG} \cdot A_{TG}} \quad (4.20)$$

The exposure range for TCC for being in the shallow decline saturation region F is:

$$\frac{(C_{store} \cdot A_{store} + C_{sense} \cdot A_{sense}) \cdot (V_{TG\_low}^* - V_{low})}{\eta} < Exposure_F < \frac{C_{store} \cdot A_{store} \cdot (V_{high} - V_{low}) + C_{TG} \cdot A_{TG} \cdot (V_{high} - V_{TG\_low})}{\eta} \quad (4.21)$$

#### 4.1.2.7. Zero gain saturation region (G)

This region starts with the onset of charge injection during the back-transfer operation. In this region, the total charge in the wells satisfies the condition:

$$Q_{STN} + Q_{STO} + Q_{TG} < Q_{total} \quad (4.22)$$

In this stage, the charge after the back transfer is constant, independent of the exposure level. Redistribution (charge sharing) occurs and the charge remaining in the pixel will be equal to  $Q_{STN} + Q_{STO} + Q_{TG}$ .

The TCC formula for this region is:

$$V_{sense}(Exposure_G) = V_{low} + \frac{A_{sense} \cdot C_{sense} \cdot (V_{high} - V_{low})}{A_{sense} \cdot C_{sense} + A_{TG} \cdot C_{TG} + A_{store} \cdot C_{store}} \quad (4.23)$$

The exposure condition for being in the zero gain saturation region G is:

$$Exposure_G > \frac{C_{store} \cdot A_{store} \cdot (V_{high} - V_{low}) + C_{TG} \cdot A_{TG} \cdot (V_{high} - V_{TG\_low})}{\eta} \quad (4.24)$$

#### 4.1.2.8. *Experimental confirmation of the TCC derivation*

Using the previously derived formulas, TCC's have been calculated for pixel#7 for different TG voltages. The figures below show a good agreement between the calculated and the measured TCC's. There are certain differences in the linearity in various regions of the curve as well as small differences around the border between regions. This is probably due to secondary effects neglected by the simple model used in the calculations. An important factor to consider in a more precise calculation is the capacitive coupling between the sensing gate and other parasitic capacitances in the pixel. This will include the capacitance of the preamplifier gate, the capacitance of the drain/source terminal of the preset transistor, the fringing capacitance between the edge of the sensing well and the substrate, etc.

Applying the previously derived equations it can be seen that for different voltages and photogate areas, different regions of the TCC can be missing. For instance if the TG well is deep (see  $V_{TG} = 3.5V$  on the calculated curve), the charge sharing region C can start very early and the imager might never achieve the maximum saturation level. In this case region F will also be very extended.

If the TG well is deeper than the sensing well (see  $V_{TG} = 2V$  on the calculated curve), the output will be zero until enough charge will be collected to fill up part of the TG well so that charge can now “overflow” to the sensing well region. If on the other hand the TG well is very shallow (see  $V_{TG} = 5V$  on the calculated curve), both the charge

sharing regions (C and F) will be missing and region B and D will connect (the same is true for E and G in this case).

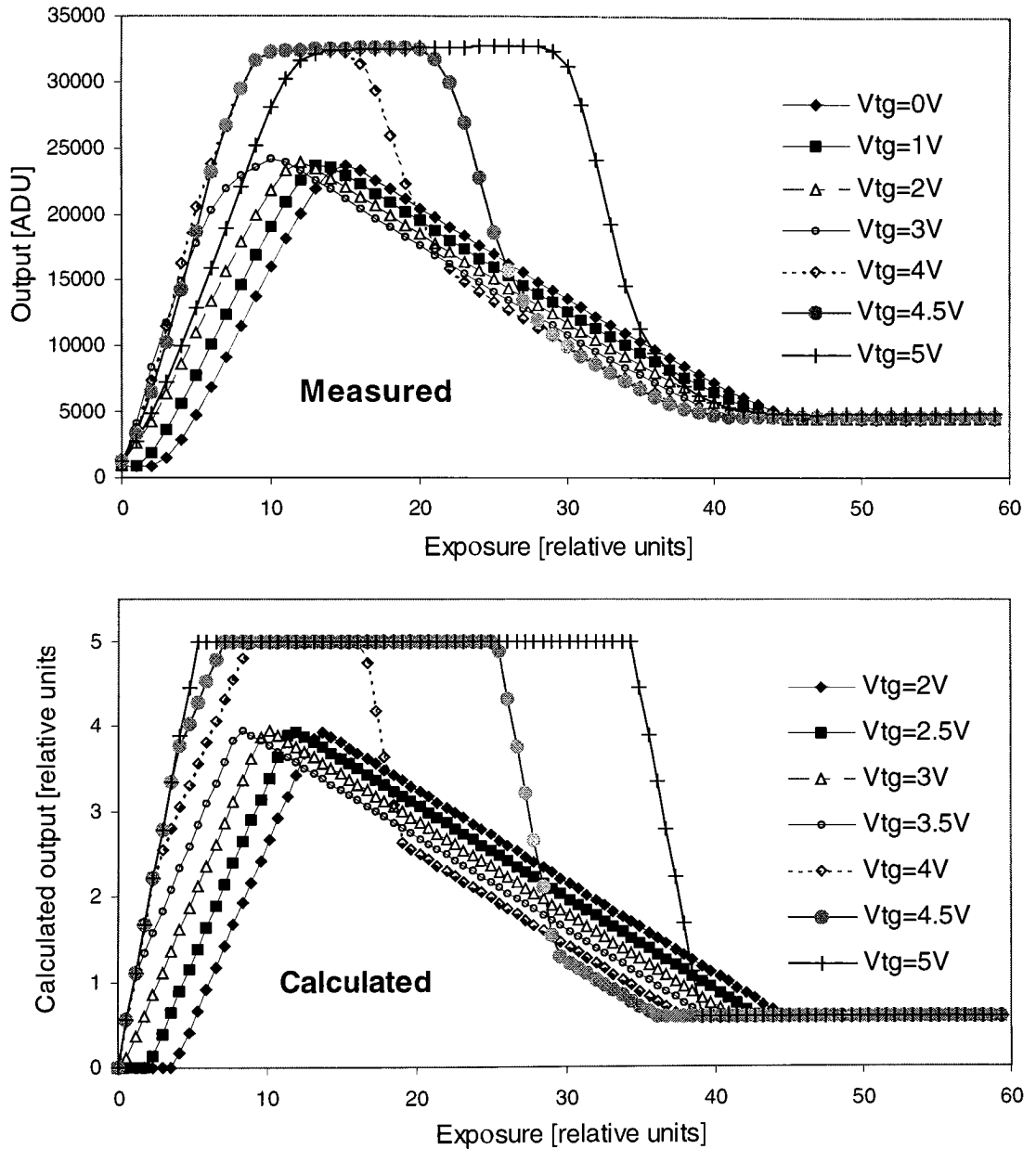


Figure 4.8 TCC plots of pixel#7 for various TG voltages

## 4.2. Gain and noise

An example of the *Mathcad* program used for the pixel preamplifier noise estimation is presented in *Appendix 2*. The simulation was done on a CDS noise simulation set up by Joe Carbone of CIDTEC based on a noise power spectrum calculation by J. M. Pimbley and G. J. Michon<sup>32</sup>. The noise of the readout chain has been simulated for a bandwidth of 30KHz and a value of 20-40 $\mu$ V at the output of the chip was obtained. Since there is an operational amplifier in a noninverting configuration with a gain of 28.4 inserted between the imager output and the A/D converter, the estimated noise becomes 5-10 A/D units.

An important thing to observe from the mean variance curve (Figure 4.9) is that the intercept of the linear fit and the value of the variance in the dark are not the same. Usually the first is higher (noisier).

	Gain [ADU/electron]	Readout noise [ADU]	Simulated readout noise [ADU]	Intercept noise [electrons]	<b>Readout noise [electrons]</b>
Pixel#1	1.046	7.4	5 to 10	6	<b>7</b>
Pixel#2	0.810	7.4	5 to 10	17	<b>9</b>
Pixel#3	0.751	7.6	5 to 10	19	<b>10</b>
Pixel#4	0.726	6	5 to 10	21	<b>8</b>
Pixel#5	0.929	6.4	5 to 10	19	<b>7</b>
Pixel#6	1.045	7.5	5 to 10	22	<b>7</b>
Pixel#7	1.271	7	5 to 10	7	<b>5.5</b>
Pixel#8	0.993	7	5 to 10	32	<b>7</b>
<b>Average</b>	<b>0.946</b>	<b>7.04</b>	<b>5 to 10</b>	<b>18</b>	<b>7.56</b>

Table 4.3 Outline of the gain and readout noise measurement results at  $-30^{\circ}\text{C}$

While measuring the variance of the pixel output in the dark, the surface states are partially depleted, and it can be assumed the charge in the potential wells is partially frozen. No charge transfer means that the uncertainty in the amount of electric charge in the potential wells after injection does not appear in the output. It means that in dark conditions the noise measured does contain a negligible amount of injection noise.

The above assumption is strengthened by the fact that the noise value measured in the dark (expressed in ADU) doesn't vary much with the pixel geometry, the preamplifier is the same for all pixel configurations (same readout noise expected), and in the dark the photon shot noise is zero. If the injection noise were present in the dark, the noise would be larger for larger area photogates.

The intercept of the linear fit is calculated based on output values obtained with exposure so that the surface states get filled up and the injection noise starts to manifest itself.

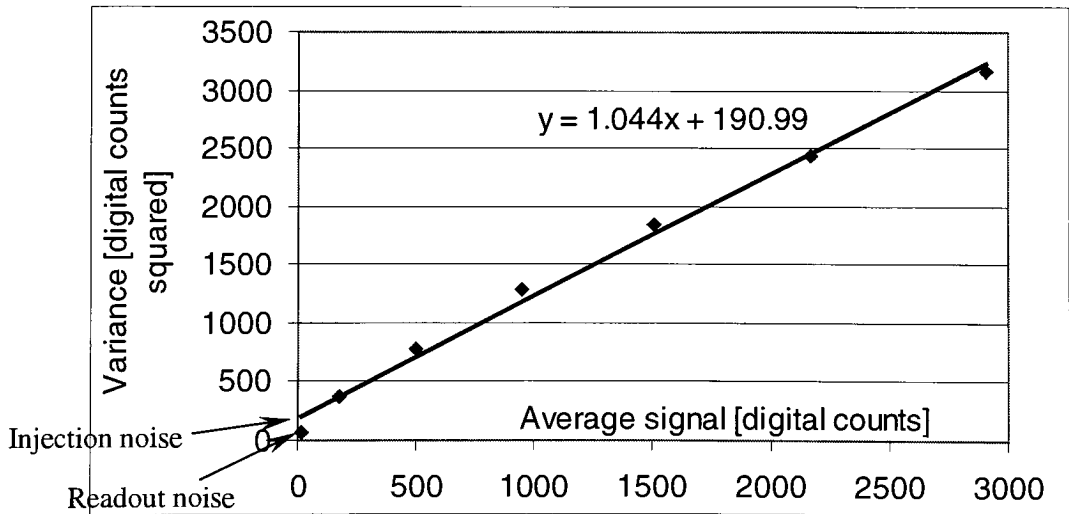


Figure 4.9 Mean-variance plot for pixel#5. Readout noise and the injection noise are indicated



The noise in the dark is in the order of 5-10 electrons and the noise calculated based on the linear fit intercept is in the order of 6-32 electrons depending on the pixel geometries (for higher the overall area of the electrodes there is a tendency for higher intercept noise).

Figure 4.9 exemplifies the readout noise and the injection noise for pixel#5. Figure 4.10 shows the value of the photogate area together with the dark noise and intercept noise for various pixels. We can see that the readout noise is not too dependent of the photogate area while the intercept noise is. There is one exception, which is pixel#7. This is probably due to the fact that the storage gate of this pixel has a very contorted shape, which makes the transfer for very low charge level difficult (no fringing fields – section 1.2.3). Therefore the injection noise is masked.

We can draw the conclusion that the injection noise is dominant for the pixels with large photogate area whereas the preamplifier readout noise is dominant for the ones with small photogate area.

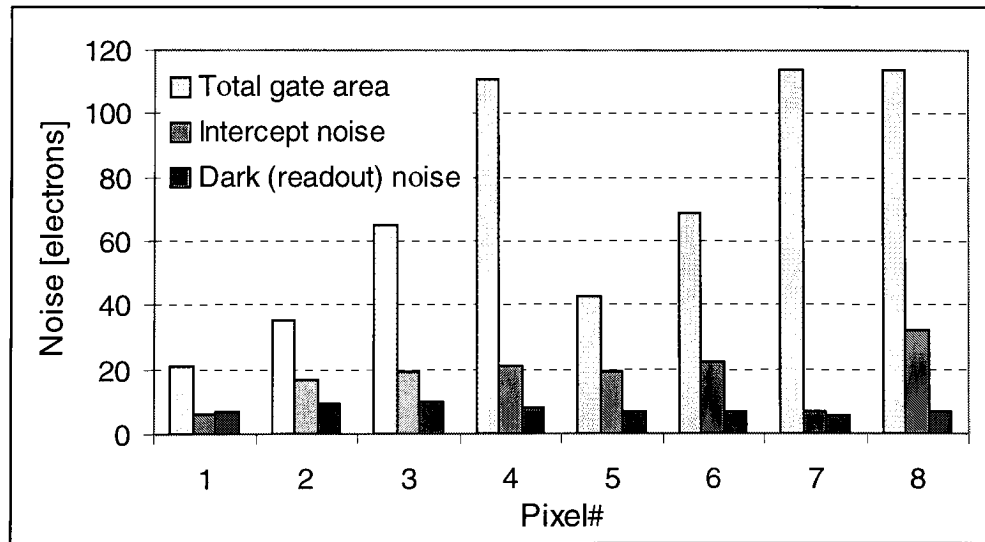


Figure 4.10 The dependence of the intercept and dark noise of the total photogate area

Two very important observations have to be made here. The first one is that the injection noise can be eliminated either by using a buried channel device, or by reading the array using correlated triple sampling (CTS). In the latter case the array is read out using correlated double sampling (CDS) right after injection, in the dark, before the integration operation. This value is stored in a digital memory for each pixel separately, and then it is extracted from the final post-integration CDS readout value. The memorized value represents the bias charge after the injection, and contains all the injection noise. This method is used in photodiode arrays where simple CDS techniques are not effective in removing the reset (kTC) noise.

Another important observation is that the readout noise can be reduced by using multiple, nondestructive readout<sup>21</sup>. The noise will decrease with the square root of the number of readout operations. This means that by using CTS and reading the array nondestructively 50 times, noise figures below one electron can be obtained. Running the array at cryogenic temperatures could further reduce the noise.

### 4.3. Nonlinearity

Nonlinearity can be caused by the charge-to-voltage conversion process in the sensing well, or by the preamplifier.

As far as the charge-to-voltage conversion process in the sensing well is concerned nonlinearity can arise from several factors. Only two of them will be mentioned here.

At low light levels the reduced charge transfer efficiency in surface channel devices can be a source of nonlinearity (section 1.2.3). At high charge levels (close to saturation) the charge sharing process between the sensing gate and the storage gate can produce a sharp drop in linearity (section 4.1.2). As seen in section 4.1.2 the higher the TG voltage the less pronounced this effect is. However too high a voltage on the transfer gate can diminish the charge transfer efficiency, hence worsening the linearity in the lower region of the TCC.

	Lowest nonlinearity (from Figure 3.6)	Fraction of output range for which the lowest linearity occurs	Preamplifier nonlinearity	Total photogate area [ $\mu\text{m}^2$ ]	Ratio of store_gate_area/sense_gate_area
Pixel#1	0.5 %	40 %	0.05 %	21.1	1
Pixel#2	0.4 %	80 %	0.15 %	35.5	1
Pixel#3	1.0 %	65 %	0.25 %	64.7	1
Pixel#4	1.4 %	60 %	0.4 %	110.7	1
Pixel#5	1.1 %	40 %	0.1 %	42.9	4.027778
Pixel#6	1.7 %	62 %	0.1 %	68.9	7.638889
Pixel#7	1.9 %	65 %	0.2 %	114.1	6.458333
Pixel#8	1.7 %	62 %	0.2 %	116.1	6.597222

Table 4.4 An outline of nonlinearity for different pixel configurations

The two mechanisms mentioned above could be observed in Figure 3.6 where all the nonlinearity curves have a high value at low charge level. This corresponds to charge transfer inefficiency. After passing through a minimum all the curves start going up which corresponds to entering in the stage of charge sharing.

Looking at Table 4.4 we can see that the nonlinearity of the preamplifier is much smaller (3 to 9 times smaller) than the nonlinearity of the preamplifier over the same range.

Another conclusion we can draw from the same table is that the higher the ratio of the storage gate area over the sensing gate area, the higher the nonlinearity. To explain this, we can think in terms of potential well areas and depths. This means the higher the storage gate area over sensing gate area ratio, the less charge per unit area is needed under the storage gate after the back-transfer operation to produce a given output. At low charge levels fringing fields (section 4.1.2) dominate the charge transfer. The fringing fields for some pixels are reduced due to the length of the storage gate and its area (section 4.1.2.1 and Table 4.2). The above-mentioned results point again that the main nonlinearity mechanism involved at low charge level is the charge transfer inefficiency.

## 4.4. Fixed pattern noise and shading

Nowadays, fixed pattern noise is the most serious drawback in APS devices. The fixed pattern noise results presented here show quite large values. During the measurement it was observed that both FPN and shading are affected by biasing conditions, and there is an obvious effect of the pixel geometry on both parameters. Besides obvious charge transfer efficiency in pixels with very long gates, which makes the FPN dependent of biasing conditions, it seems that this parameter is not very dependent on the pixel configuration. For a given manufacturing process, the larger the geometries the more uniform the lithographic definition of their area and shape. For a given process it is therefore expected the FPN to vary inversely proportional with pixel size. In our case, at 27mm pixel size, levels around 1% r.m.s. FPN are measured.

In order to make a usable image, the r.m.s. FPN value has to be smaller than the photon shot noise. For 388x16 Orbit device the measured FPN is actually several times larger in value than the photon shot noise so there is the need for FPN correction.

### 4.4.1. FPN correction

#### 4.4.1.1. *Background*

There are many ways of compensating the FPN but in this dissertation, we will concentrate only on off-chip computation-based image processing techniques, which are very effective in scientific imaging, where large image processing resources are available. These methods would allow one to better understand FPN mechanisms and reveal ways of FPN compensation circuit design.

Any transfer characteristic curve can be approximated as a polynomial expansion. The higher the order of the polynomial equation describing the approximation, the better the FPN and shading removal. It will be proven in section 4.4.1 that a first order (linear) correction can improve the FPN and shading performance by almost an order of magnitude by bringing all the transfer characteristic curves of the pixels together in two different points. The computation resources needed to do this process are much less than in the case of higher order corrections. The more linear the pixels the better the linear correction. But even for pixels with very nonlinear transfer characteristics a linear FPN correction will perform very well if the pixels are “nonlinear in the same way”. This means that adequate linear equations (customized for each pixel) can bring the transfer characteristics close to a unique “master TCC”.

As a consequence a useful metrics for characterizing the FPN linear “correctability” was introduced (section 3.9) as the nonlinearity fixed pattern noise NLFPN.

Suppose we have a number of pixels and we want to correct for FPN. Before attempting to do any correction we have to make sure other noise sources (especially the scene shot noise which dominates for high level signals) are eliminated from equations. As a consequence all the numerical manipulations discussed here are done on frame averages (16 frames).

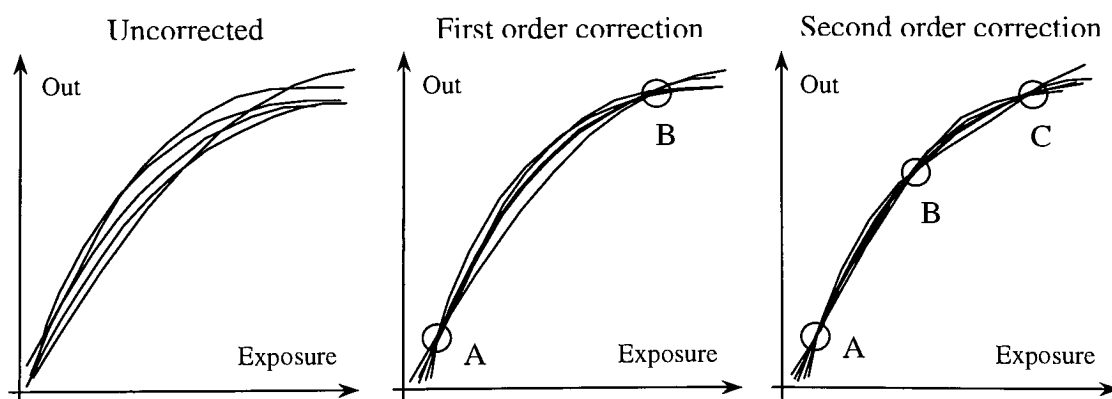


Figure 4.11 Example of FPN correction

Figure 4.11 exemplifies the correction mechanism. A bundle of transfer characteristics are brought together in two different points by using a linear (first order) correction, and in three different points by using a quadratic correction. Let's call the exposure levels at which the perfect FPN correction is done, *cardinal correction points* (CCP's).

#### 4.4.1.2. Algorithm

Let's assume there is a 400-pixel frame. Considering an  $n$ -order correction, the general equation describing the correction is:

$$C_{corrected}(x) = A_n C^n(x) + A_{n-1} C^{n-1}(x) + \dots + A_0 \quad (4.25)$$

If we pick up a number of  $n+1$  different levels of exposure (CCP's) between 0% and 100% of the input range,  $n+1$  frames of data are acquired. The procedure is repeated  $m$  times (10-50).  $n+1$  average frames are obtained in which each pixel is an average of  $m$  values. There are now available  $400 \times (n+1)$  points of data:

$$C_p(x_i) \quad \text{where } p = (1, 400) \quad \text{and } i = (0, n) \quad (4.26)$$

Calculating the frame average in the CCP's we obtain  $n+1$  numbers:

$$C_{corrected}(x_i) = \text{Average}[C_p(x_i)] \quad \text{where } i = (0, n) \quad (4.27)$$

With this data, a linear system can be formed and solved for each pixel ( $p$  from 0 to 400):

$$C_{corrected}(x_i) = A_{np} C_p^n(x_i) + A_{(n-1)p} C_p^{n-1}(x_i) + \dots + A_{0p} \quad \text{where } i = (0, n) \quad (4.28)$$

The result ( $A_{np}, A_{(n-1)p}, \dots, A_{0p}$ ) can be written as an  $(n+1)$ -size vector. It is different for every pixel and can be used as coefficients in equation (4.1) to do the pixel correction.

First order and second order correction examples are discussed in the next section.

#### **4.4.1.3. Results and discussion**

An important issue is choosing the CCP's where the actual correction coefficients are calculated. A solution would be to pick up more correction points and try to isolate different combinations of CCP out of them.

The darker the scene the lower the photon shot noise in the scene therefore the FPN is more of a problem at low light levels. In order to improve the image quality it is important to pick the first CCP at very low light levels if not at zero exposure.

Results of a linear and quadratic correction respectively are presented in the graphs below. The CCP is picked in the origin (dark). At high levels of signal both corrections perform satisfactory. At low light levels however the quadratic correction performs about two times better due to an additional CCP chosen at low light levels (16.6% of the input range).

In order to improve the correction even further, a higher order correction can be chosen. There solution is computational extensive. For a linear correction there is the need for one multiplication and one addition per pixel. For a quadratic correction there is the need for four multiplications a three additions. Can different coefficients (than the ones given in the section 4.4.1.2) be found to increase the effectiveness of a certain order correction?



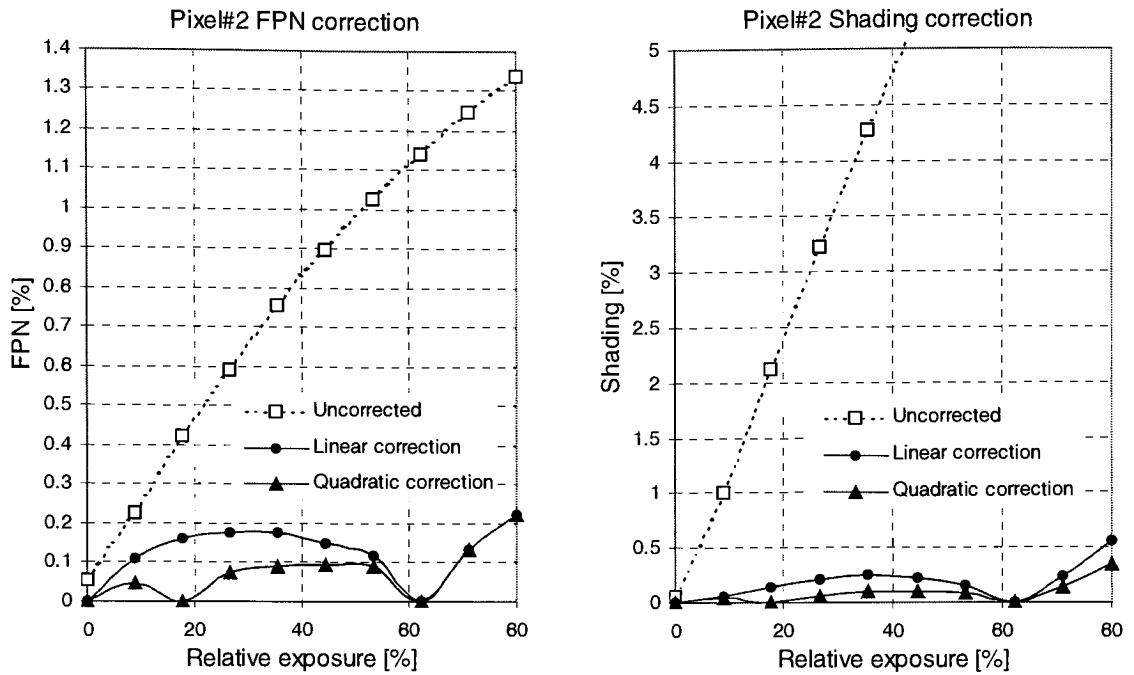


Figure 4.12 Fixed pattern noise and shading plots for first order correction and second order correction respectively

#### 4.4.1.4. Improving correction efficiency - equalized FPN correction

Let's consider a second order correction. In this case a bundle of transfer characteristics are brought together in in three different cardinal correction points (CCP's). Looking at Figure 4.11 it can be seen that the FPN of the array after correction is cancelled in three CCP's (0%, 16% and 66%).

In the dark, the photon shot noise goes to zero so that it is not a bad idea to cancel FPN completely in that point but for the next two CCP's it would be useful to distribute the FPN more evenly rather than cancel it sharply in one point. This will increase the value of the FPN in the correction point but it is expected to decrease the value of this parameter in the neighboring correction points. The ideal is not to have a constant FPN

across the input range but one which is as small as possible but proportional to the photon shot noise. This will give the fixed pattern noise a minimum visibility in the image.

Let's consider equation (4.1) applied for the quadratic case:

$$C_{corrected}(x) = A_2 C^2(x) + A_1 C(x) + A_0 \quad (4.29)$$

If we pick up a number of  $n$  different levels of exposure between 0% and 80% of the input range,  $n$  frames of data are acquired. In our particular case  $n = 10$ , which is larger than 3, the number of CCP's for a quadratic correction. The procedure is repeated  $m$  times (16 in our experiment).  $n$  average frames are obtained in which each pixel is the average of  $m$  values.

$$C_p(x_i) \quad \text{where } p = (1, 400) \quad \text{and } i = (0, n-1) \quad (4.30)$$

Calculating the frame average in all the  $n$  cases we obtain  $n$  numbers:

$$C_{corrected}(x_i) \quad \text{where } i = (1, n) \quad (4.31)$$

Selecting three CCP's out of  $n$  exposure levels, a linear systems can be formed and solved for each pixel ( $p$  from 0 to 400):

$$C_{corrected}(x_i) = A_{2p} C_p^2(x_i) + A_{1p} C_p(x_i) + A_{0p} \quad \text{where } i = (0, n-1); i \in \{CCP\} \quad (4.32)$$

This is the regular procedure described in section 4.4.1.2.

In order to switch to a equalized FPN algorithm we will make  $C_p$  a linear combination of its neighbors. So for each pixel in the array we can write the equation:

$$C_{p\_distributed}(x_i) = w_{i0} \cdot C_p(x_0) + w_{i1} \cdot C_p(x_1) + \dots + w_{i(n-1)} \cdot C_p(x_{n-1}) \quad (4.33)$$

where  $p = (1,400)$  and  $i = (0, n-1)$  and  $x_i \in \{CCP\}$

Or in the matrix form the equation above can be written for each pixel:

$$\begin{pmatrix} C_{p\_distributed}(x_a) \\ C_{p\_distributed}(x_b) \\ C_{p\_distributed}(x_c) \end{pmatrix} = \begin{pmatrix} w_{a0} & w_{a1} & \dots & w_{a(n-1)} \\ w_{b0} & w_{b1} & \dots & w_{b(n-1)} \\ w_{c0} & w_{c1} & \dots & w_{c(n-1)} \end{pmatrix} \times \begin{pmatrix} C_p(x_0) \\ C_p(x_1) \\ \dots \\ C_p(x_{n-1}) \end{pmatrix} \quad (4.34)$$

where  $p = (1,400)$  and  $x_a, x_b, x_c \in \{CCP\}$

Let's call the matrix  $[W]$  the matrix of distributed coefficients.

The three frame averages in the CCP's are calculated as in the regular algorithm:

$$C_{corrected}(x_i) = Average[C_p(x_i)] \quad (4.35)$$

where  $i = (0, n-1)$  and  $x_i \in \{CCP\}$

With the data, a linear systems can be formed and solved for each pixel ( $p$  from 0 to 400):

$$C_{corrected}(x_i) = A_{2p} C_{p\_distributed}^2(x_i) + A_p C_{p\_distributed}(x_i) + A_{0p} \quad (4.36)$$

where  $i = (0, n-1)$  and  $x_i \in \{CCP\}$

The system can be written in matrix form for every pixel:

$$\begin{pmatrix} C_{corrected}(x_a) \\ C_{corrected}(x_b) \\ C_{corrected}(x_c) \end{pmatrix} = \begin{pmatrix} C_{p\_distributed}^2(x_a) & C_{p\_distributed}(x_a) & 1 \\ C_{p\_distributed}^2(x_b) & C_{p\_distributed}(x_b) & 1 \\ C_{p\_distributed}^2(x_c) & C_{p\_distributed}(x_c) & 1 \end{pmatrix} \times \begin{pmatrix} A_{2p\_distributed} \\ A_{1p\_distributed} \\ A_{0p\_distributed} \end{pmatrix} \quad (4.37)$$

where  $p = (1,400)$  and  $x_a, x_b, x_c \in \{CCP\}$

The result (matrix  $[A_{p\_distributed}]$ ) can be used as coefficients in equation (4.5) to do the correction for each individual pixel.

The question arises about the way one chooses the right matrix of distributed coefficients  $[W]$  to calculate the  $C_{p\_distributed}(x_i)$ . A rigorous approach is not given here since this would dependent on the target FPN curve. However, an empirical way based on trial and error is shown as example. In this dissertation an FPN characteristic similar but proportionally smaller to the photon shot noise curve is targeted.

#### 4.4.1.5. *Equalized quadratic FPN correction - example*

The imager is being uniformly illuminated with 10 different levels of exposure from 0% to 90% of the saturation level. The procedure is repeated 16 times and 10 average frames are computed for each light level. For any of these frames each pixel value will be the average of 16 pixel values taken at the same light level so that the effect of temporal noise is minimized. Three CCP's are selected:  $x_0, x_2, x_7$  (0%, 16.7% and 66.7%).

The following matrices of distributed coefficients were used in the second order correction and distributed second order correction respectively.

Figure 4.13 contains a plot of the FPN when both versions of second order correction were applied. The result in both cases is few times smaller than the photon shot noise, which means that the FPN would be visually undetectable in both cases.

$$(W_{regular\_correction}) = \begin{pmatrix} 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 \end{pmatrix}$$

$$(W_{distributed\_correction}) = \begin{pmatrix} 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & \frac{30}{55} & \frac{8}{55} & \frac{8}{55} & \frac{15}{55} & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & \frac{30}{95} & \frac{20}{95} & \frac{10}{95} & \frac{10}{95} & \frac{30}{95} \end{pmatrix}$$

Figure 4.14 shows the effect of two different second order FPN correction algorithms on the output of a 300-pixel sequence while illuminated with an arbitrary scene (in this case there is a progressive rounded shadow in the middle of the column).

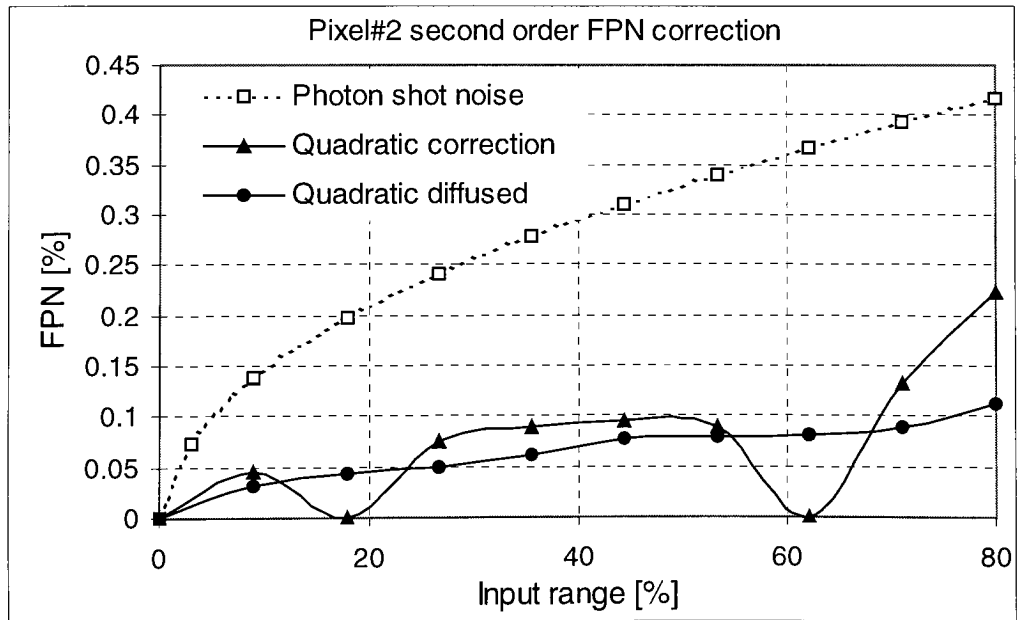


Figure 4.13 Two different types of quadratic correction for the same type of pixel

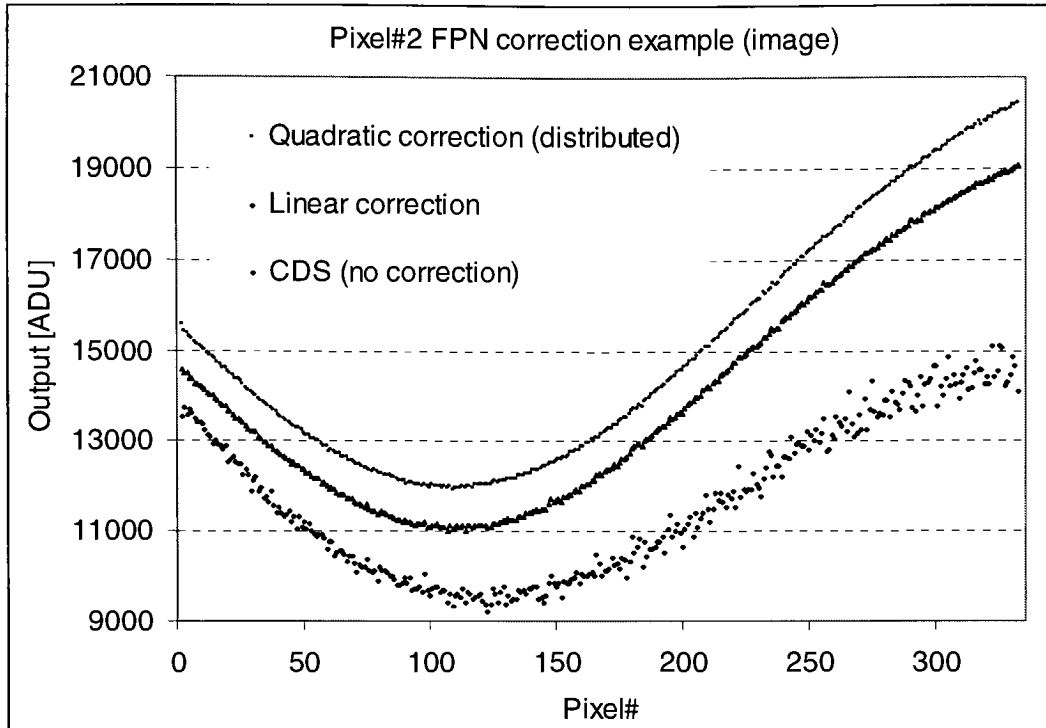


Figure 4.14 Effects of two different FPN correction techniques on an arbitrary image

## Chapter 5. Conclusions

### 5.1. Research objective

The purpose of the research presented in this dissertation was investigating novel types of image sensors as possible successors to charge coupled devices (CCD's) in scientific applications.

From the beginning, the AP-CID was the main target of this research, since it promised to offer the advantages of the CID (section 1.3.2.4) and active pixel sensors (section 1.5.3) combined. This research addresses five main aspects:

- The first aspect was finding a suitable architecture that would allow successful fabrication of an array, which would preserve the aforementioned advantages.
- The second aspect was reducing the high readout noise-level specific to passive CID's and bring it in the range of noise specific to scientific CCD's. Typical figures for present CID's are around 300 to 1000 electron r.m.s. readout noise. About one order of magnitude noise reduction (below 20 electrons r.m.s.) was targeted.
- The third aspect was measuring and understanding the performance of the new device in order to offer solutions for further improvement of the design. The main field of application targeted was space-based astronomy.

## 5.2. Performance review

### 5.2.1. Summary of measured parameters

The table below contains a summary of the measured performance of the 388x16 Orbit AP-CID array. Based on this data a final analysis is done and guidelines for an upgraded design are given in section 5.2.2.

	Pixel#1	Pixel#2	Pixel#3	Pixel#4	Pixel#5	Pixel#6	Pixel#7	Pixel#8
Maximum output signal	197 mV	395 mV	691 mV	971 mV	247 mV	247 mV	494 mV	494 mV
Nonlinearity @ output range	0.5 % @40%	0.4% @80%	1.0% @65%	1.4% @60%	1.1 % @40%	1.7% @80%	1.9% @65%	1.7% @60%
Temporal read noise [e]	7	9	10	8	7	7	5.5	7
Inject noise [e]	Negligible	17	19	21	19	22	7	32
Gain [ADU/e]	1.05	0.81	0.75	0.73	0.93	1.05	1.27	0.99
Full well cap. [electrons]	35,000	91,000	176,000	252,000	52,000	47,000	72,000	93,000
Dynamic range	4,970	9,950	17,350	30,660	7,660	6,540	13,140	12,920
QE @ [550nm]	1.66	2.94	3.89	3.48	3.15	3.68	3.71	4.58
QE @ [300nm]	2.03	3.15	2.75	1.55	3.43	2.17	1.51	2.15
FPN	1%	1.3%	1.8%	0.8%	1%	1.8%	1%	1.3%
Shading	3%	7%	9%	6%	2%	4%	2.5%	4%
NFPN	0.15%	0.1%	0.2%	0.3%	0.15%	0.4%	0.2%	0.2%
Dark current at room temp [h/s]	3700	4500	5250	3670	5940	5950	5650	6600
Pixel preamp. V-gain	0.729	0.729	0.729	0.729	0.729	0.729	0.729	0.729

Table 5.1 Performance review for the 388x16 Orbit AP-CID array



## **5.2.2. Comparison of various pixel architectures – guidelines for an upgraded design**

### **5.2.2.1.    *The maximum output signal***

The maximum output signal is strongly dependent on the size of the sensing gate. The storage gate area has an initial role which means beyond a certain size (which is larger than the sensing gate) the maximum output range is independent of this parameter.

The maximum output is limited to about one order of magnitude less than the voltage swing on the storage gate during charge transfer. This is due to parasitic capacitance in the pixel connected to the sensing gate which “pin” the voltage on the sensing gate. The voltage pinning has both a good effect (decreasing the nonlinearity), and a bad effect (decreasing the dynamic range of the pixel).

It is important to mention that about 1V is the maximum signal swing on the sensing gate (pixel#4), and it is not very dependent on the supply voltages. This means that even in deep submicron manufacturing processes, where the power supply voltages are low this device will retain a good performance. The performance parameter is expected to drastically decrease only below 2-3V supply voltage.

### **5.2.2.2.    *The nonlinearity***

The linearity is very good for the first two pixels. This parameter is strongly affected by charge transfer. The charge sharing may affect nonlinearity for low TG voltages.

It is very important to keep the storage and sensing gates relatively short and strait otherwise serious nonlinearity issues might arise. If larger full well capacities are required, it is recommended that few short/straight gates be connected in parallel.

#### **5.2.2.3.    *The temporal read noise***

The readout noise is excellent for all the pixels. Provided the array is read slowly (tens of kHz pixel frequency) the read noise is mildly dependent on the pixel geometry.

The salient point to highlight here is that a small sensing gate is expected to yield a higher conversion gain hence a better noise figure. However a smaller sensing gate is more sensitive to the voltage pinning due to the parasitic capacitance associated with this gate. The two effects described work against each other and the gain seems to be not very affected by the size of the sense gate.

The preamplifier design is not critical. This result was known from the Mathcad simulation and confirmed experimentally. The preamplifier should be designed strong enough to be able to satisfy speed requirements.

#### **5.2.2.4.    *The injection noise***

This type of noise is larger than the preamplifier read noise. The level of this type of noise is proportional to the total photogate area. This noise component can be removed by using correlated triple sampling when digital image processing resources are available.

To completely eliminate this type of noise while operating the imager in CDS readout mode, the device must be build in a buried channel technology.

#### **5.2.2.5.    *The gain***

The gain is not very dependent on the pixel configurations since the smaller the sensing gate the more effect the parasitic capacitance will have on the maximum voltage swing of this gate.

#### **5.2.2.6.    *The full well capacity***

This parameter is strongly dependent on the size of the sensing gate. The larger the sense gate the higher the full well capacity.

#### **5.2.2.7.    *The dynamic range***

Since dynamic range is mere the ratio of the full well capacity and the minimum temporal noise, this parameter is strongly dependent on the size of the sensing gate. The larger the sense gate, the higher the full well capacity. For some pixels (#3, #4 and #8) this parameter has excellent values, exceeding four orders of magnitude.

While designing an AP-CID imager with very good dynamic range attention should be paid to the fact that this parameter and linearity vary in opposite ways (but not obeying a simple, linear relationship) with the sensing gate size. The designer must look for a trade off.

#### **5.2.2.8.    *The quantum efficiency (QE)***

Quantum efficiency has low values for this particular imager. This is partly due to the high doping concentration of the pixel substrate and partly due to the active electronics in the pixels. The electronics is made of reverse biased PN junctions, which act as charge drains.

QE in near UV is almost as good as maximum QE for these pixels since there is a vast area in the pixel uncovered by polysilicon photogates.

To improve this parameter, the photosensitive area has to be built on a lightly doped silicon region. Careful pixel design can also improve QE.

#### **5.2.2.9.    *The fixed pattern noise and shading***

FPN and shading have relatively high values. Most of the problem comes from nonuniformities in the charge-to-voltage conversion process within the pixel. It was observed that the larger the photogate area, the smaller the FPN at very low light levels. A way of reducing this parameter is by increasing pixel size.

Methods for off-chip correction were demonstrated (section 4.4.1)

#### **5.2.2.10.   *The dark current***

About 200nA/second at room temperature and an increase of an octave for each 7.9°C was observed. These are typical numbers for surface channel CID processes. The dark current performance can be improved by running the array at low temperatures.

### 5.2.2.11. An improved pixel layout

An improved pixel layout is presented below. The pixel has three groups of photogates in parallel. The gates are short and straight rendering a good transfer efficiency hence a better linearity at low charge levels. This way the quantum efficiency, full well capacity and dynamic range are high (as measured in pixel with large electrode areas) without compromising linearity.

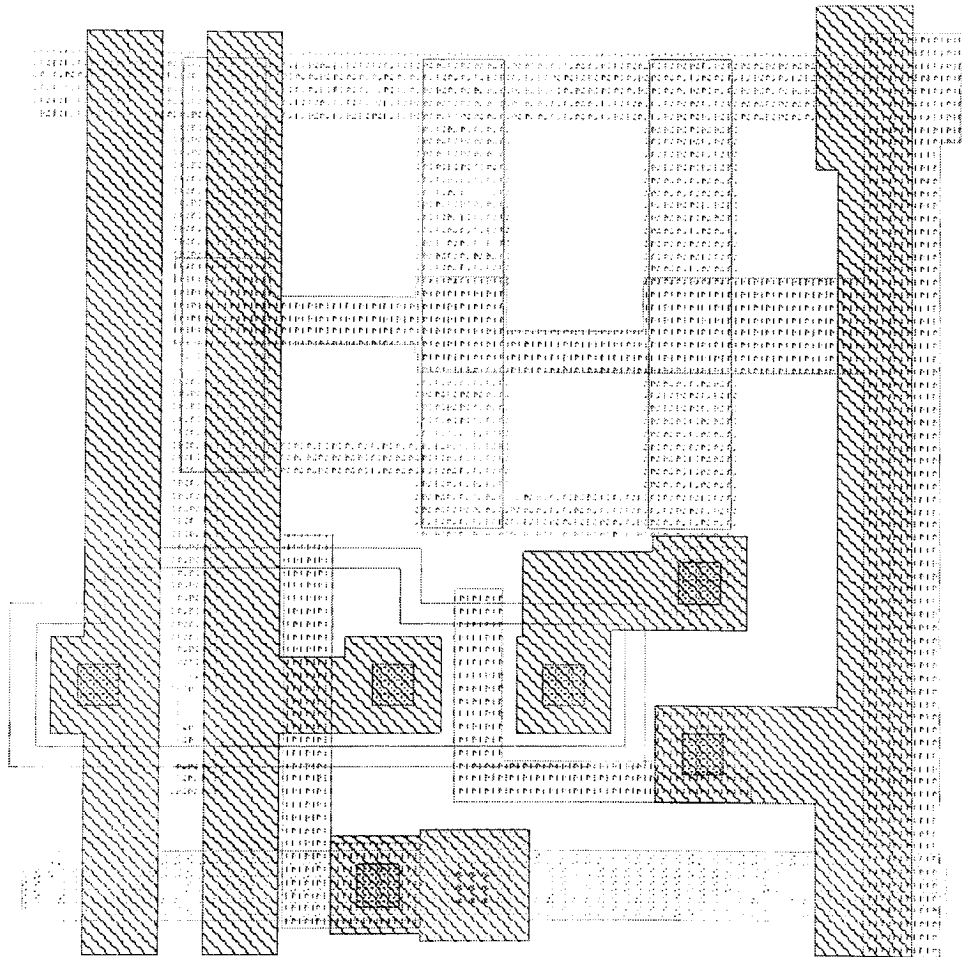


Figure 5.1 An improved pixel layout having photogates in parallel

The amplifying transistor is wider providing more pinning effect, a lower noise, and lower output impedance.

### **5.2.3. Goals accomplished**

As a result of the work described in this dissertation, a new type of sensor, the AP-CID, has been developed. This device retains most of the positive features of both the CID imager (random readout, non-destructive readout, antiblooming, increased UV sensitivity, radiation tolerance, low power consumption, low manufacturing price) and the CCD imager (low noise, high dynamic range) and lacks most of the drawbacks of the previously mentioned devices.

The research goals as stated in section 5.1 have been met. A functional array architecture was created (section 2.2.2). The noise performance of this array is excellent (section 4.2). The device was fully measured (Chapter 3), characterized and suggestions for improvement were formulated (Chapter 4).

# Appendix

## Noise calculation for the 32x32 Mosis AP-CID

### 1. **Source Follower Transistor Input Parameters**

$W := 1.5$	gate width (in $\mu\text{m}$ )
$L := 0.5$	gate length (in $\mu\text{m}$ )
$I_{\text{sat}} := 1 \cdot 10^{-5}$	drain current (DC average) from SPICE simulation (in A)
$f_{\text{corner}} := 10^6$	corner frequency of the 1/f noise (in Hz), <b>estimated</b> one order of magnitude larger than the typical value measured at CIDTEC for the ORBIT surface chan- nel PMOST.

### 2. **Calculation of the Transconductance of the Source Follower**

$\mu_n := 400$	electron mobility (in $\text{cm}^2/\text{V}\cdot\text{sec}$ )
$t_{\text{ox}} := 0.7 \cdot 10^{-6}$	gate oxide thickness (in cm)
$\epsilon := 3.5 \cdot 10^{-13}$	permittivity of silicon dioxide (in F/cm)
$\beta := \frac{\mu_n \cdot \epsilon}{t_{\text{ox}}} \cdot \frac{W}{L}$	parameter of the transistor (in F/V.s)
$g_m := \sqrt{2 I_{\text{sat}} \cdot \beta}$	transconductance in saturation region (in S)

### 3. **Determination of the FET Power Density Spectrum**

$k := 1.38 \cdot 10^{-23}$	Boltzmann's constant (in J/K)
$\gamma := 1$	a noise parameter typically between 0.67 and 1 (the worst case)
$T := 150$	absolute temperature (in K) - cryogenic operation

The Johnson noise power spectrum for an FET in the source follower configuration is uniformly distributed in the spectrum and it is given by the following formula:

$$S_{\text{johnson}} := \frac{4 \cdot k \cdot T \cdot \gamma}{g_m} \cdot 10^{18} \quad (\text{in nV}^2/\text{Hz})$$

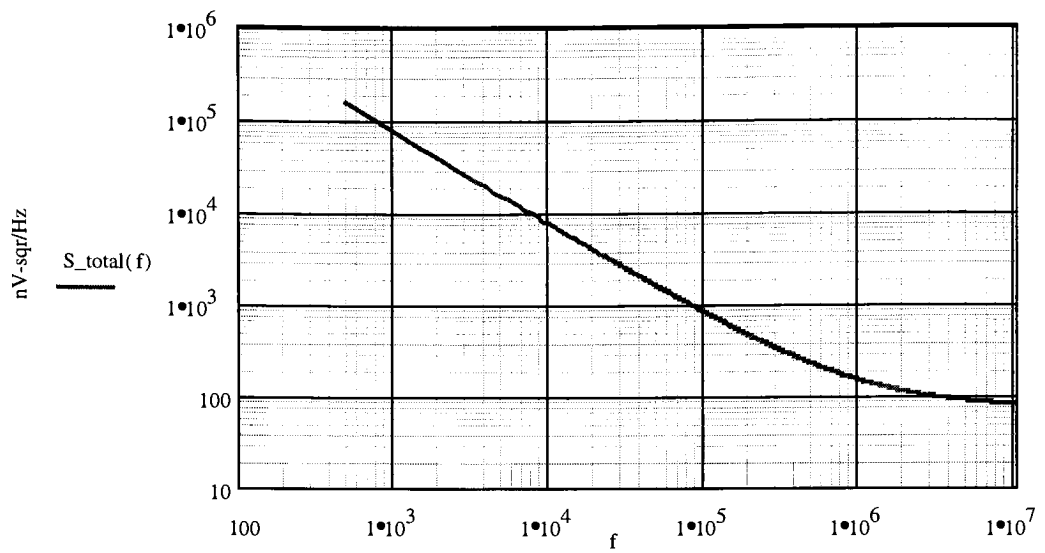
$$S_{\text{johnson}} = 75.586 \quad (\text{in nV}^2/\text{Hz})$$

The power spectrum of the 1/f noise (flicker noise) can be characterized by the following formula:

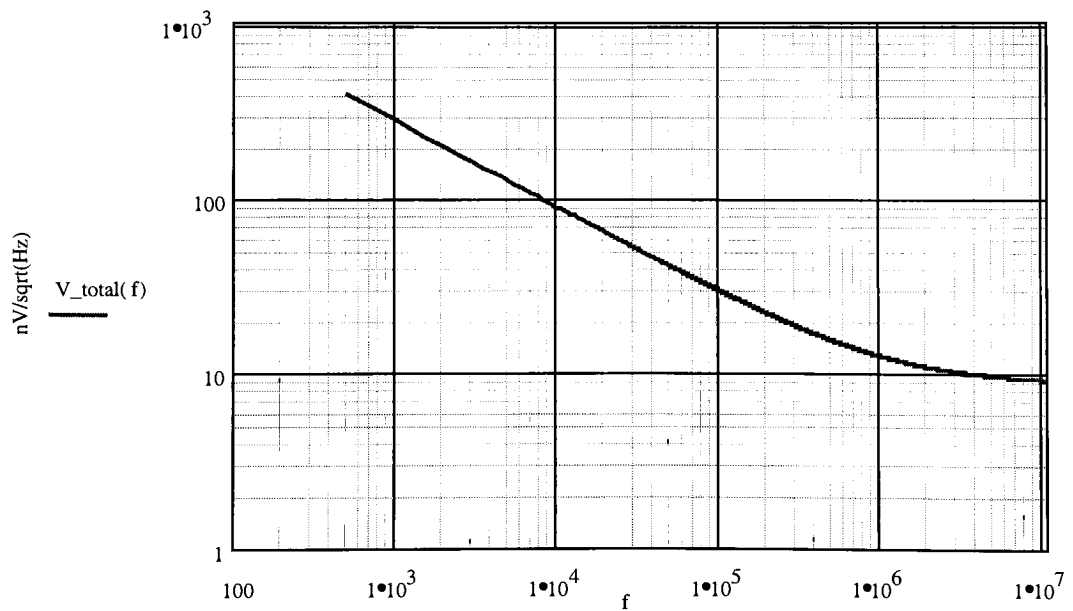
$$f := 500, 1000, \dots, 1 \cdot 10^7 \quad \text{frequency (in Hz)}$$

$$S_{\text{flicker}}(f) := S_{\text{johnson}} \cdot \frac{f_{\text{corner}}}{f} \quad \text{flicker noise power spectrum (in nV}^2/\text{Hz)}$$

$$S_{\text{total}}(f) := S_{\text{flicker}}(f) + S_{\text{johnson}} \quad \text{total noise power spectrum (in nV}^2/\text{Hz)}$$



$$V_{\text{total}}(f) := \sqrt{S_{\text{total}}(f)} \quad \text{total noise voltage function (nV}/\sqrt{\text{Hz}})$$



As it can be seen from the above graph, the pixel preamplifier noise input spectrum is  $1/f$  dominated through 1MHz, and correlated-double-sampling could be employed as means to optimize the overall noise performance.



#### 4. **Correlated Double Sampling (CDS) Process**

CDS provides a means to reduce the KTC noise and 1/f noise in analog signal processing. As Pimbley and Michon demonstrated [1], noise suppression is dependent upon electronics bandwidth. For the case of a switched clamp and sampling circuit, they derived the following expression for the output power density spectrum:

$$S_{out}(f) := 4 \cdot \left[ \frac{\sin\left(\pi \cdot \frac{f}{f_p}\right)}{\pi \cdot \frac{f}{f_p}} \right]^2 \cdot \sum_{n=-\infty}^{\infty} \sin(f - n \cdot f_p) \cdot (\sin(\pi \cdot \lambda \cdot (f - n \cdot f_p)))^2$$

where  $S_{out}(f)$  = noise output power density function

$f_p$  = pixel rate

$f$  = frequency

$S_{in}(f)$  = input power density function

$\lambda$  = time between clamp and sample actions

The series is convergent only if the input power spectrum is limited.

#### 5. **Limiting the Input Power Spectrum**

The amplifier input noise power spectrum is not finite. Therefore the electronics bandwidth must be limited in order to obtain a convergent noise output power spectrum series. This will be accomplished by inserting a capacitor in parallel to the output bus of the imager, thus limiting the output of the preamplifier. This is equivalent to limiting the power spectrum at the input of the CDS circuit, i.e.  $\{S_{in}(f)\}$  can be expressed as the product of the preamplifier input noise power spectrum  $\{S_{total}(f)\}$ , the square of the DC gain of the amplifier chain  $\{A\}$  and the magnitude of the filter transfer function squared  $\{|H_{filter}(f)|^2\}$ .

$$S_{in}(f) := S_{total}(f) \cdot A^2 \cdot |H_{filter}(f)|^2$$

$A := 0.85$

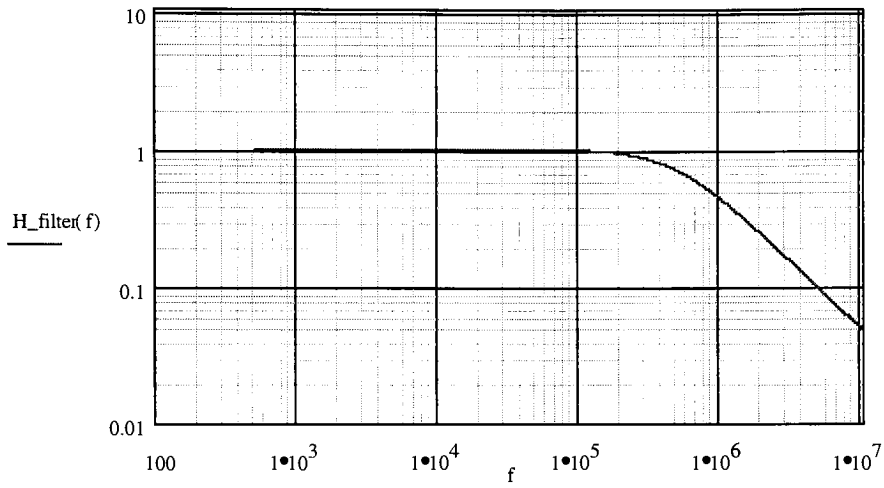
preamplifier DC gain (dimensionless)

In order to realize an optimum noise reduction, the filter should exhibit a step response of one half the pixel duration  $\{f_p\}$ . Mathematically the filter transfer function can be modelled as a single pole RC low-pass filter. Assuming a 10 MHz pixel rate the RC constant must be smaller or equal to 100 nanosecond. A compromise has to be reached between the total noise after the CDS stage and the signal attenuation (3dB in voltage for RC=100ns).

$f_p := 10^6$  pixel frequency (Hz)

$RC := \frac{1}{3} \cdot \frac{1}{f_p}$  low pass filter time constant (s)

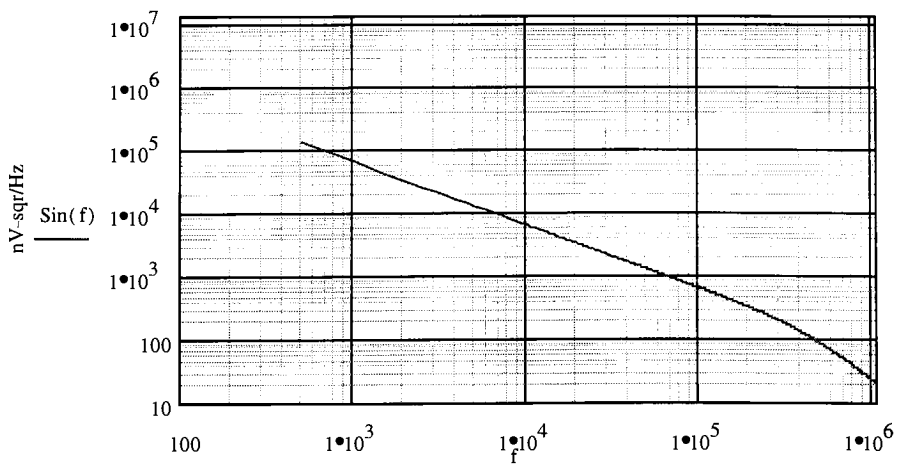
$H_{\text{filter}}(f) := \frac{1}{\sqrt{1 + (2 \cdot \pi \cdot f \cdot RC)^2}}$  the absolute value of the low-pass filter transfer function (dimensionless)



Low Pass Filter Characteristic Function

The resulting power spectrum after low-pass filtering becomes:

$\text{Sin}(f) := S_{\text{total}}(f) \cdot A^2 \cdot \frac{1}{1 + (2 \cdot \pi \cdot f \cdot RC)^2}$  power spectrum into the CDS circuit (in  $\text{nV}^2/\text{Hz}$ )



Power Spectrum into the CDS Circuit

## 6. The Output Power Density Spectrum

The expression for the output density spectrum is calculated below assuming the following parameters:

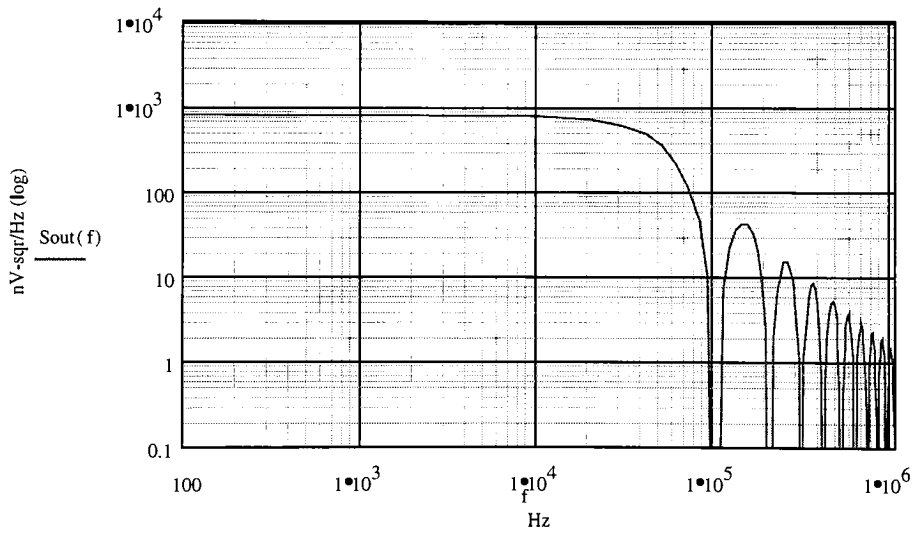
$N := 10$  the number of significant terms in the series expansion (dimensionless)

$\lambda := \frac{1}{2} \cdot \frac{1}{f_p}$  time interval (shorter than the pixel period) between clamp and sample actions

$f_p := 10^5$  pixel frequency (Hz)

$f := 1, 10000, 10^7$

$$S_{out}(f) := 4 \cdot \left[ \frac{\sin\left(\pi \cdot \frac{f}{f_p}\right)}{\pi \cdot \frac{f}{f_p}} \right]^2 \cdot \sum_{n=-N}^N \sin(f - n \cdot f_p) \cdot (\sin(\pi \cdot \lambda \cdot (f - n \cdot f_p)))^2 \quad \left( \frac{nV^2}{Hz} \right)$$



Integrated Noise Power Spectrum

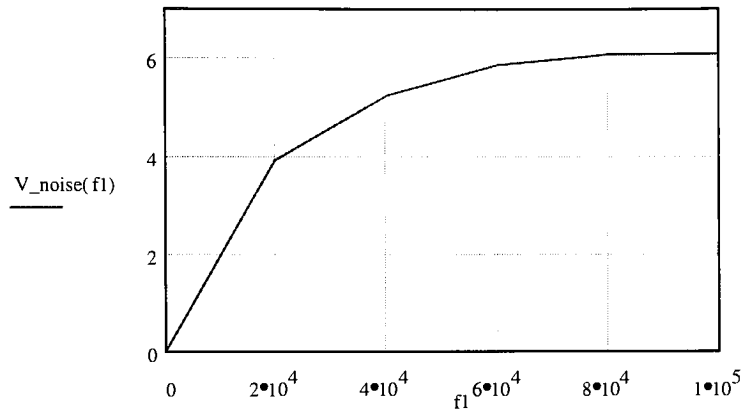
## 7. The Total Noise Power

The total output noise power is obtained by integrating the output of the noise power density spectrum over the bandwidth of interest. The integral will be performed only over positive frequencies since negative frequencies were already accounted for in the definition of the output power density function.

$$f1 := 0, 20000. \text{ fp}$$

$$P\_noise(f1) := \int_0^{f1} Sout(f) df \quad \text{total noise power (nV}^2\text{)}$$

$$V\_noise(f1) := \frac{\sqrt{P\_noise(f1)}}{1000} \quad \text{total noise output voltage (}\mu\text{V)}$$



## 9. *The Equivalent Readout Noise in Electrons*

The equivalent readout noise in electrons {Nn} can be calculated knowing the output sensitivity. The output sensitivity can be calculated by knowing the gain of the amplifier chain gain (from the simulation G=0.7) and the sensing node capacitance.

$$G := 0.7 \quad \text{the gain of the amplifier}$$

$$C\_sensing1 := 20 \cdot 10^{-15} \quad \text{the sensing node capacitance (pF) for a small area photogate pixel}$$

$$C\_sensing2 := 51 \cdot 10^{-15} \quad \text{the sensing node capacitance (pF) for a large area photogate pixel}$$

$$e := 1.6 \cdot 10^{-19} \quad \text{electronic charge (C)}$$

$$Nn1 := \frac{C\_sensing1 \cdot V\_noise(fp)}{e \cdot G} \cdot 10^{-6} \quad \text{the equivalent readout noise}$$

$$Nn2 := \frac{C\_sensing2 \cdot V\_noise(fp)}{e \cdot G} \cdot 10^{-6}$$

$$Nn1 = 1.087 \quad \text{electrons r.m.s. noise for an array having small area photogate pixel}$$

$$Nn2 = 2.773 \quad \text{electrons r.m.s. noise for an array having large area photogate pixel}$$

# References

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- <sup>1</sup> S. Morrison, "A New Type of Photosensitive Junction Device", in *Solid State Electronics*, vol. 5. 1963, pp. 485-494.
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